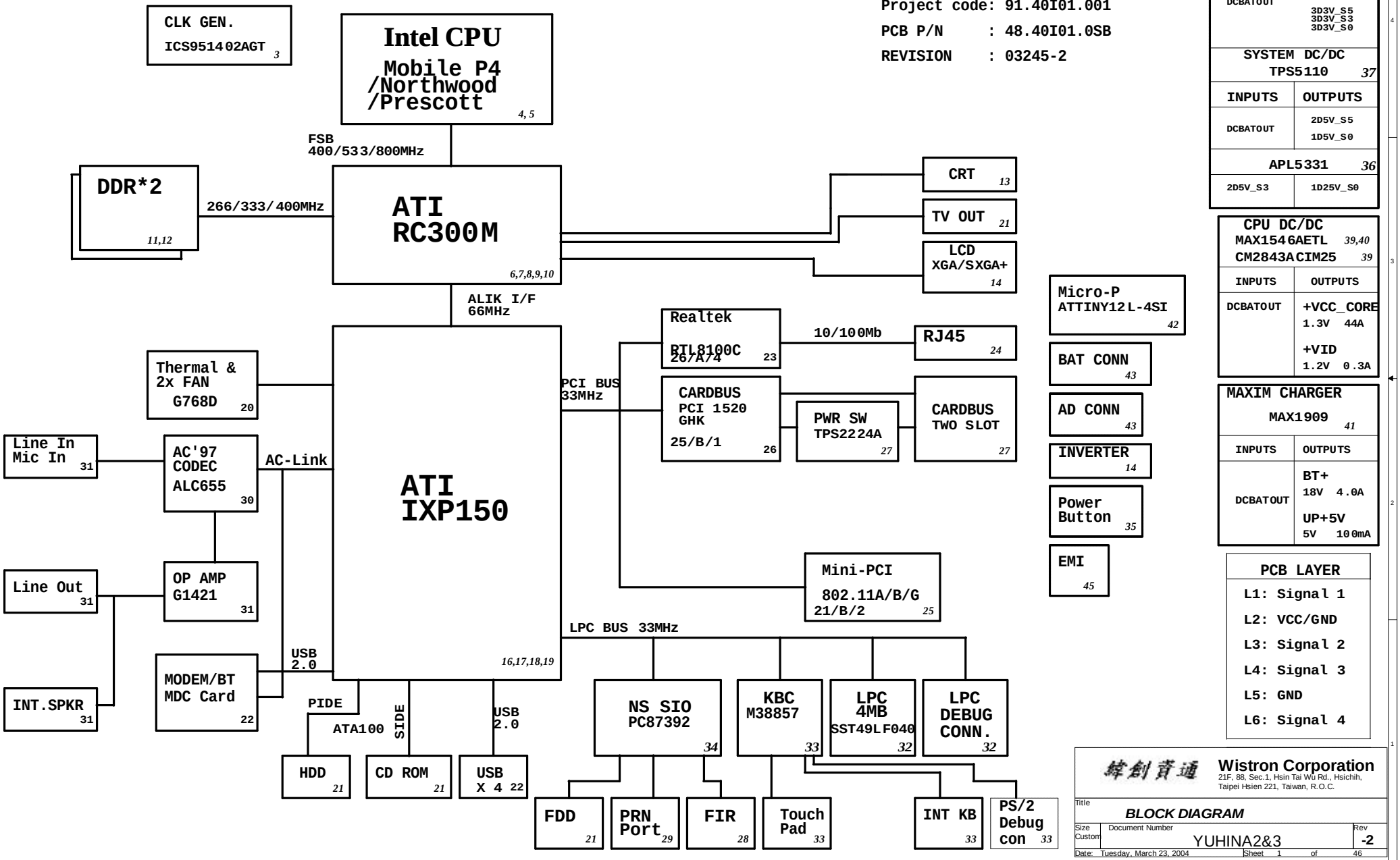
YUHINA2&3 Block Diagram

Project code: 91.40I01.001
PCB P/N : 48.40I01.0SB
REVISION : 03245-2



SYSTEM DC/DC TPS51020DBT 38

INPUTS	OUTPUTS
DCBATOUT	5V_S5 5V_S3 5V_S0 3D3V_S5 3D3V_S3 3D3V_S0

SYSTEM DC/DC TPS5110 37

INPUTS	OUTPUTS
DCBATOUT	2D5V_S5 1D5V_S0

APL5331 36

2D5V_S3	1D25V_S0

CPU DC/DC MAX1546AETL 39,40 / CM2843ACIM25 39

INPUTS	OUTPUTS
DCBATOUT	+VCC_CORE 1.3V 44A +VID 1.2V 0.3A

MAXIM CHARGER MAX1909 41

INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 4.0A UP+5V 5V 100mA

PCB LAYER

- L1: Signal 1
- L2: VCC/GND
- L3: Signal 2
- L4: Signal 3
- L5: GND
- L6: Signal 4

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Title: BLOCK DIAGRAM
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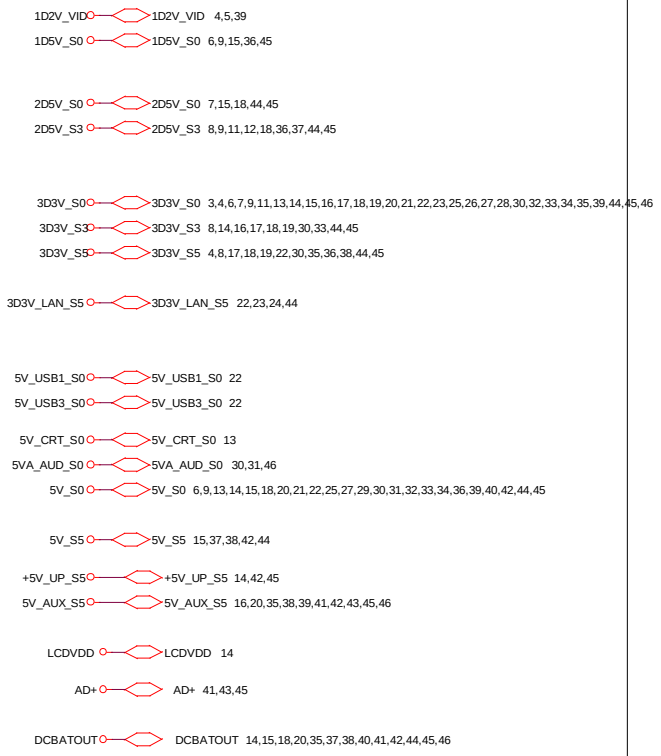
Date: Tuesday, March 23, 2004 | Sheet 1 of 46



PCI DEVICE RESOURCE ASSIGNMENT

	BUS	DEVICE	IDSEL	PCI_REQ#	PCI_GNT#	INT_IRQ#
LAN	1	5	PCI_AD26	REQ#4	GNT#4	IRQD#
CardBus	1	9	PCI_AD20	REQ#1	GNT#1	IRQB#/IRQA#
MiniPCI	1	6	PCI_AD21	REQ#2	GNT#2	IRQE#

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Title: *Table of Content / HISTORY*

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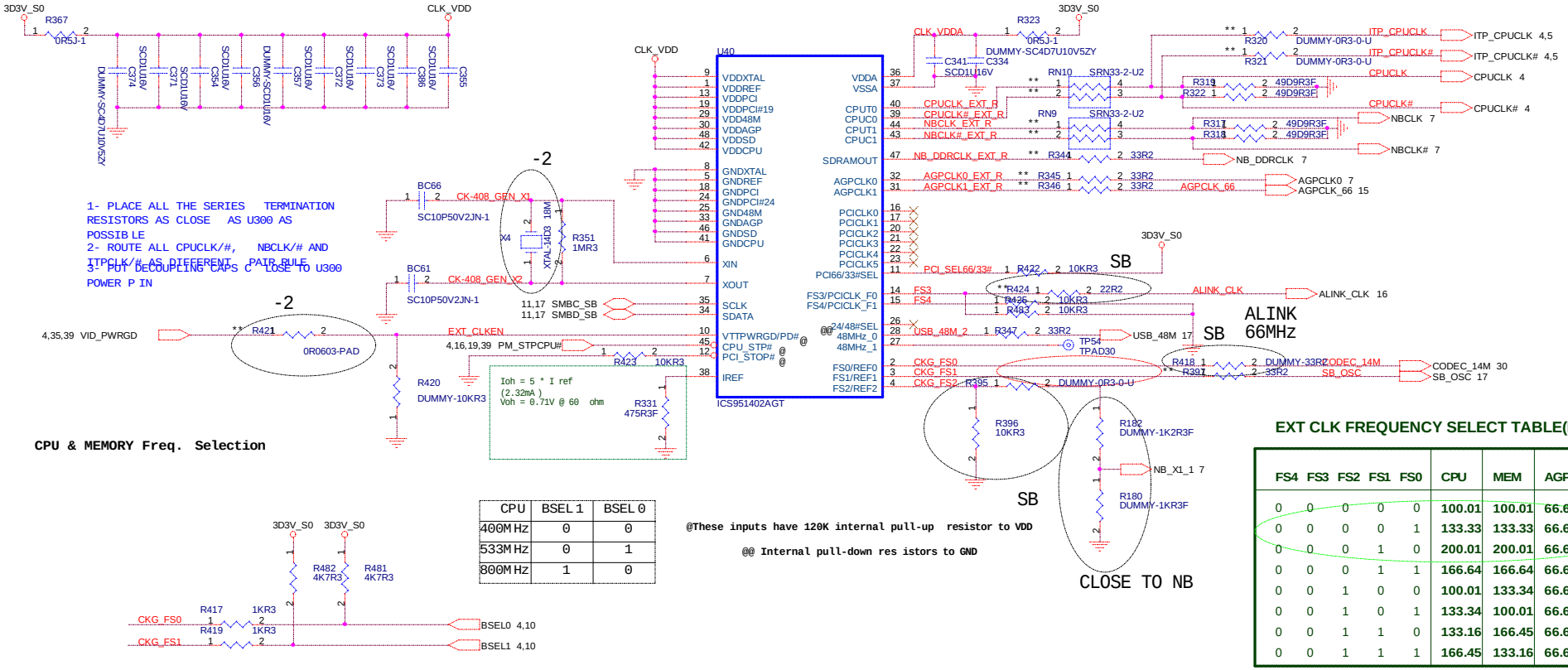

CPU & MEMORY Freq. Selection

CPU	BSEL1	BSEL0
400MHz	0	0
533MHz	0	1
800MHz	1	0

@These inputs have 120K internal pull-up resistor to VDD

@@ Internal pull-down res istors to GND

EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS4	FS3	FS2	FS1	FS0	CPU	MEM	AGP	PCI
0	0	0	0	0	100.01	100.01	66.66	33.33
0	0	0	0	1	133.33	133.33	66.66	33.33
0	0	0	1	0	200.01	200.01	66.66	33.33
0	0	0	1	1	166.64	166.64	66.66	33.33
0	0	1	0	0	100.01	133.34	66.66	33.33
0	0	1	0	1	133.34	100.01	66.66	33.33
0	0	1	1	0	133.16	166.45	66.66	33.33
0	0	1	1	1	166.45	133.16	66.66	33.33

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Title: *Clock Generator -ICS951402*

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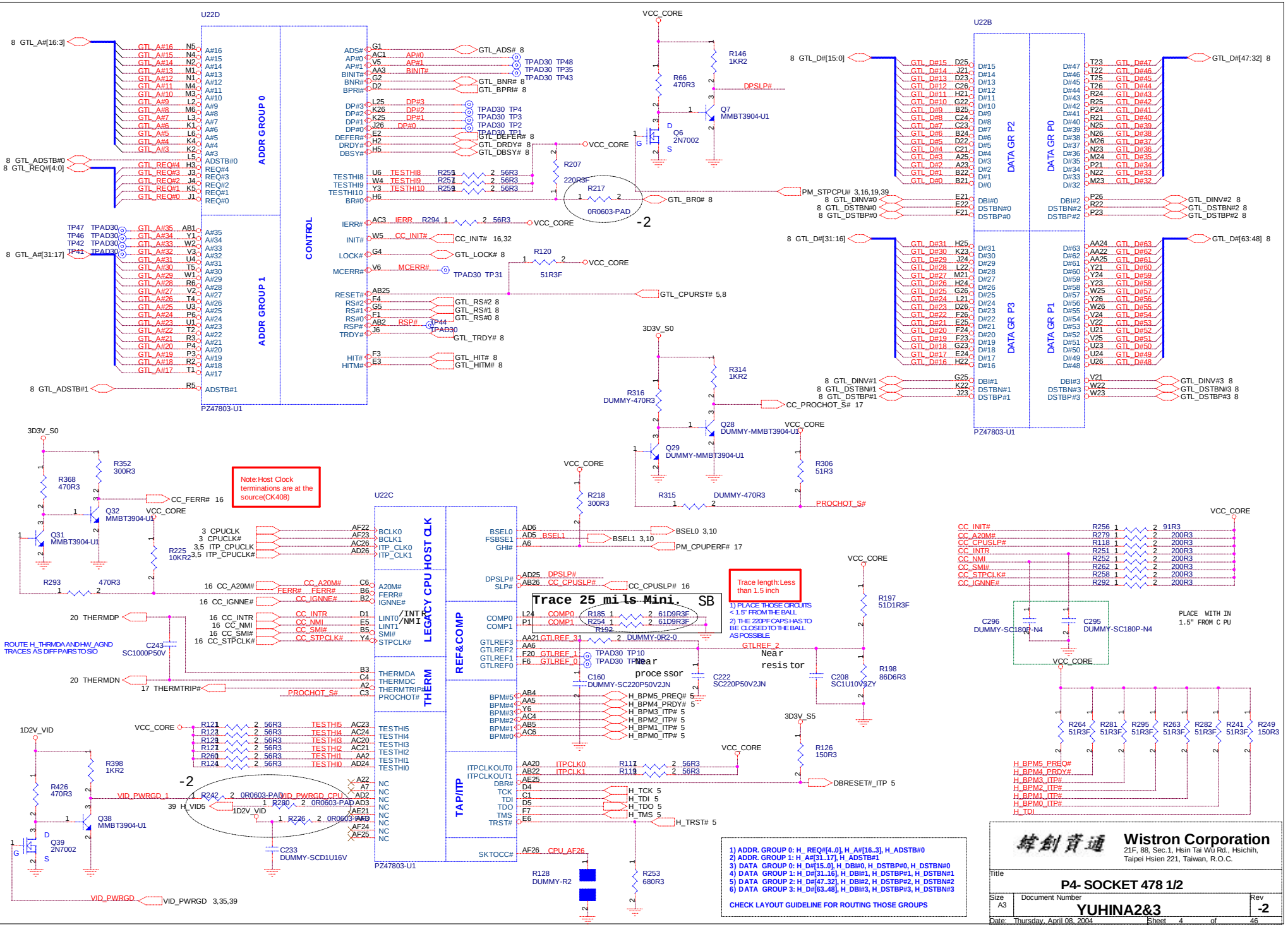
U22D
ADDR GROUP 0
ADDR GROUP 1
CONTROL
PZ47803-U1
U22C
CLK
CPU HOST
LEGACY
REF&COMP
THERM
TAP/ITP
PZ47803-U1
U22B
DATA GR P2
DATA GR P0
DATA GR P3
DATA GR P1
PZ47803-U1
Note:Host Clock terminations are at the source(CK408)
Trace length:Less than 1.5 inch
Trace 25 mils Mini.
SB
Near processor
Near resistor
PLACE WITH IN 1.5" FROM C PU
1) PLACE THOSE CIRCUITS < 1.5" FROM THE BALL.
2) THE 220PF CAPS HAS TO BE CLOSED TO THE BALL AS POSSIBLE.
ROUTE H_THRMDA AND H_AGND TRACES AS DIFF PAIRS TO SIO
1) ADDR. GROUP 0: H_REQ#[4..0], H_A#[16..3], H_ADSTB#0
2) ADDR. GROUP 1: H_A#[31..17], H_ADSTB#1
3) DATA GROUP 0: H_D#[15..0], H_DBI#0, H_DSTBP#0, H_DSTBN#0
4) DATA GROUP 1: H_D#[31..16], H_DBI#1, H_DSTBP#1, H_DSTBN#1
5) DATA GROUP 2: H_D#[47..32], H_DBI#2, H_DSTBP#2, H_DSTBN#2
6) DATA GROUP 3: H_D#[63..48], H_DBI#3, H_DSTBP#3, H_DSTBN#3
CHECK LAYOUT GUIDELINE FOR ROUTING THOSE GROUPS
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Title
P4- SOCKET 478 1/2
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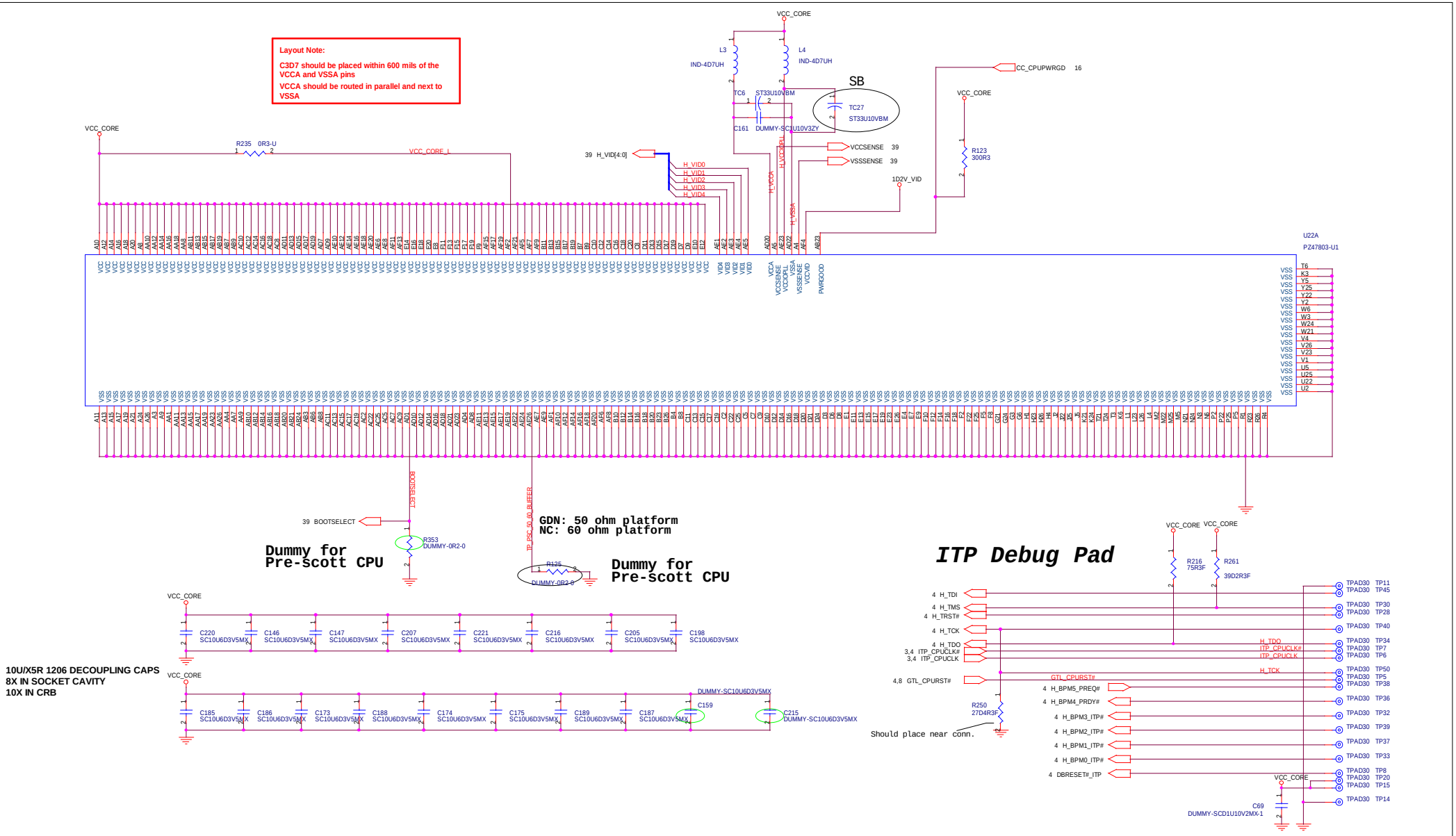
Layout Note:
C3D7 should be placed within 600 mils of the VCCA and VSSA pins
VCCA should be routed in parallel and next to VSSA
VCC_CORE
L3
IND-4D7UH
L4
IND-4D7UH
SB
TC6
ST33U10VBM
TC27
ST33U10VBM
C161
DUMMY-SC1U10V3ZY
CC_CPUPWRGD 16
R123
300R3
VCCSENSE 39
VSSSENSE 39
1D2V_VID
R235 0R3-U
VCC_CORE_L
39 H_VID[4:0]
H_VID0
H_VID1
H_VID2
H_VID3
H_VID4
H_VCCA
H_VSSA
U22A
PZ47803-U1
VCCA
VCCSENSE
VCCDQPLL
VSSA
VSSSENSE
VCCVID
PWRGOOD
VID0
VID1
VID2
VID3
VID4
BOOTSELECT
39 BOOTSELECT
R353
DUMMY-0R2-0
TP_PSC_SLAVE_BUFFER
R125
DUMMY-0R2-0
GDN: 50 ohm platform
NC: 60 ohm platform
Dummy for
Pre-scott CPU
Dummy for
Pre-scott CPU
ITP Debug Pad
R216
75R3F
R261
39D2R3F
4 H_TDI
4 H_TMS
4 H_TRST#
4 H_TCK
4 H_TDO
3,4 ITP_CPUCLK#
3,4 ITP_CPUCLK
4,8 GTL_CPURST#
4 H_BPM5_PREQ#
4 H_BPM4_PRDY#
4 H_BPM3_ITP#
4 H_BPM2_ITP#
4 H_BPM1_ITP#
4 H_BPM0_ITP#
4 DBRESET#_ITP
R250
27D4R3F
Should place near conn.
H_TDO
ITP_CPUCLK#
ITP_CPUCLK
H_TCK
GTL_CPURST#
C69
DUMMY-SCD1U10V2MX-1
10U/X5R 1206 DECOUPLING CAPS
8X IN SOCKET CAVITY
10X IN CRB
C220 SC10U6D3V5MX
C146 SC10U6D3V5MX
C147 SC10U6D3V5MX
C207 SC10U6D3V5MX
C221 SC10U6D3V5MX
C216 SC10U6D3V5MX
C205 SC10U6D3V5MX
C198 SC10U6D3V5MX
C185 SC10U6D3V5MX
C186 SC10U6D3V5MX
C173 SC10U6D3V5MX
C188 SC10U6D3V5MX
C174 SC10U6D3V5MX
C175 SC10U6D3V5MX
C189 SC10U6D3V5MX
C187 SC10U6D3V5MX
C159
DUMMY-SC10U6D3V5MX
C215
DUMMY-SC10U6D3V5MX
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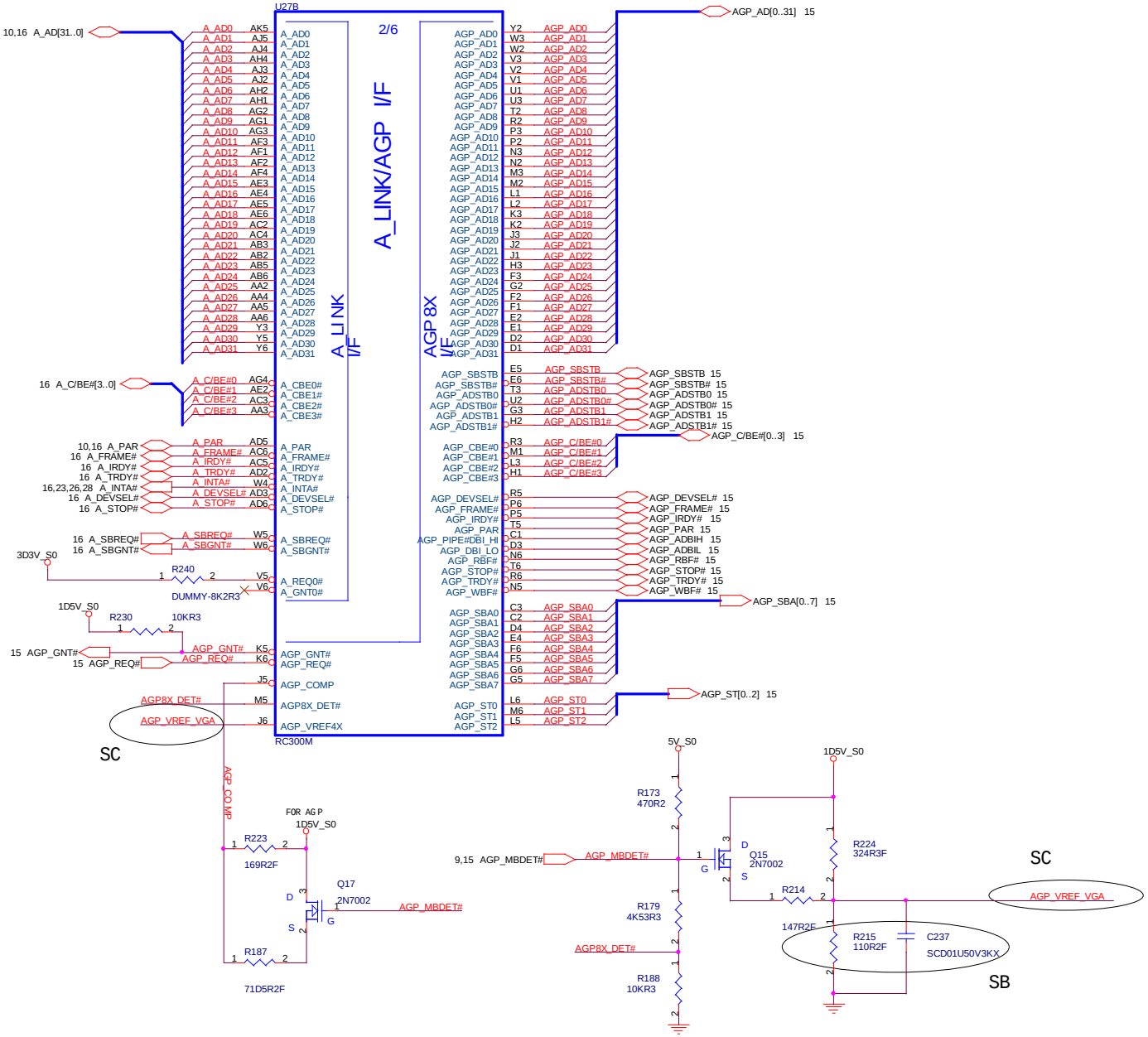

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Title: NB-A_LINK+AGP I/F		
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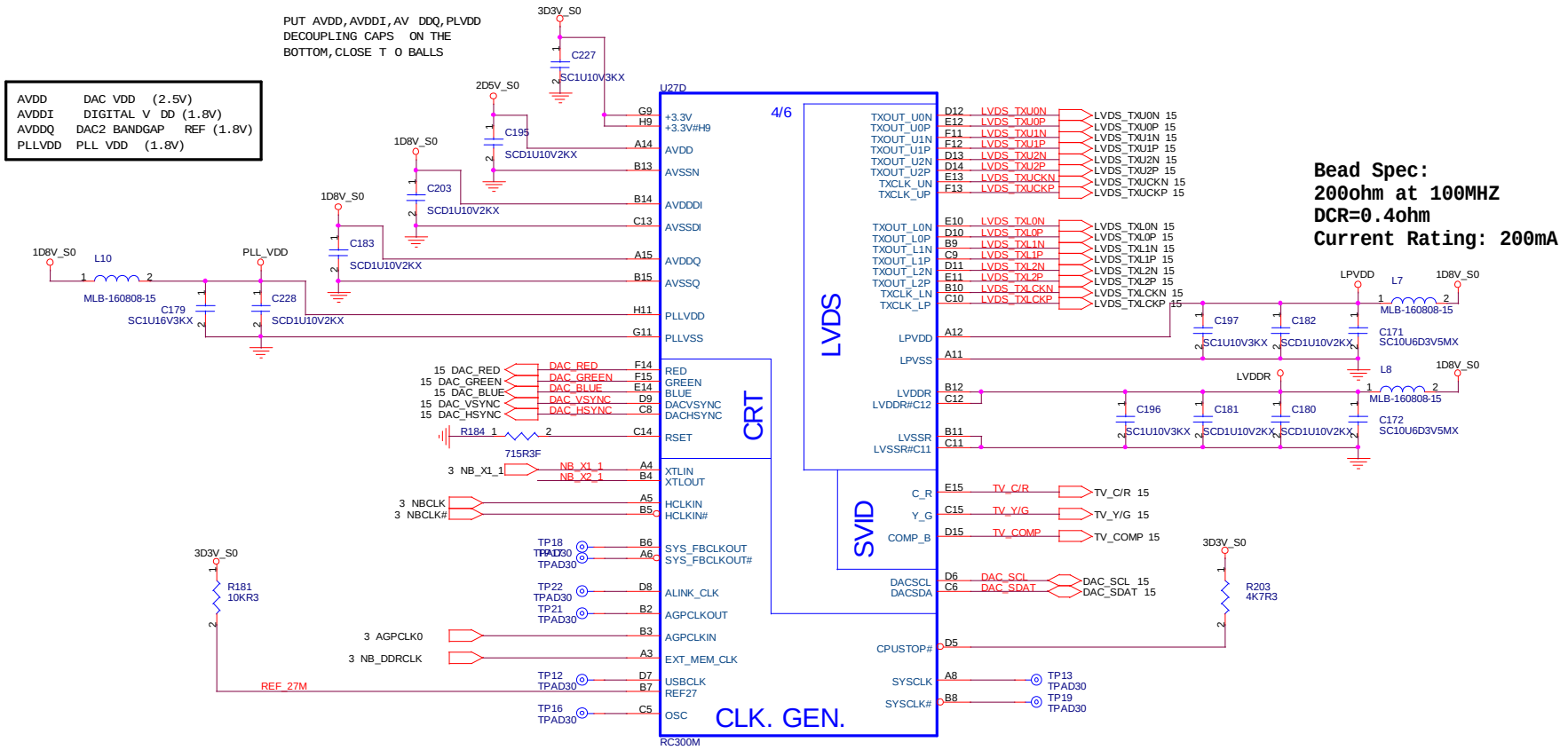

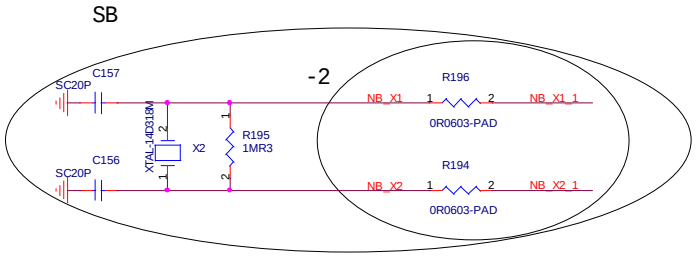

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Title: NB-VIDEO I/F &CLK GEN			
Size: A3	Document Number: YUHINA2&3	Rev: -2	
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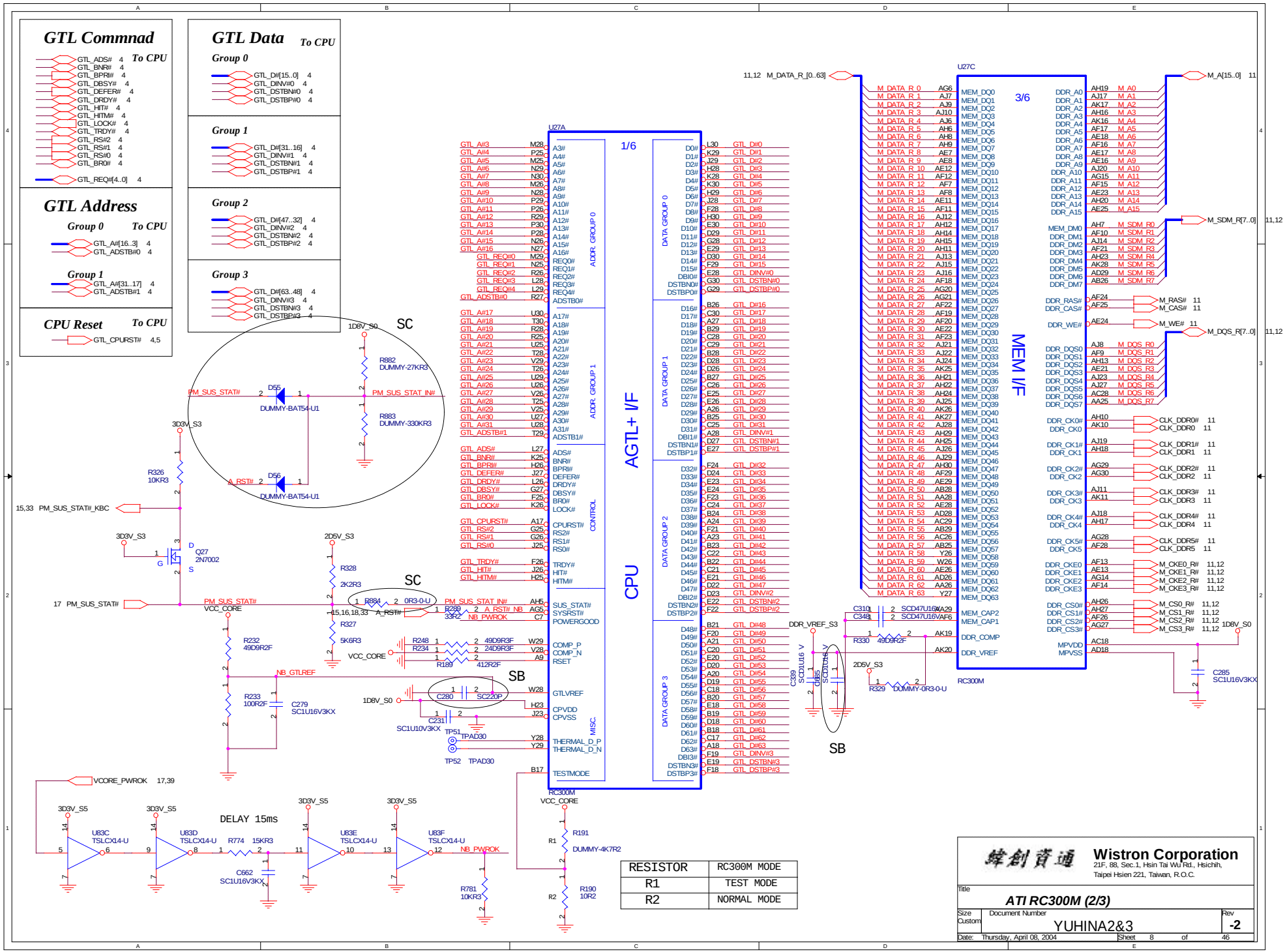
GTL Commnad
To CPU
GTL_ADS# 4
GTL_BNR# 4
GTL_BPRI# 4
GTL_DBSY# 4
GTL_DEFER# 4
GTL_DRDY# 4
GTL_HIT# 4
GTL_HITM# 4
GTL_LOCK# 4
GTL_TRDY# 4
GTL_RS#2 4
GTL_RS#1 4
GTL_RS#0 4
GTL_BR0# 4
GTL_REQ#[4..0] 4
GTL Address
Group 0
To CPU
GTL_A#[16..3] 4
GTL_ADSTB#0 4
Group 1
GTL_A#[31..17] 4
GTL_ADSTB#1 4
CPU Reset
To CPU
GTL_CPURST# 4,5
GTL Data
To CPU
Group 0
GTL_D#[15..0] 4
GTL_DINV#0 4
GTL_DSTBN#0 4
GTL_DSTBP#0 4
Group 1
GTL_D#[31..16] 4
GTL_DINV#1 4
GTL_DSTBN#1 4
GTL_DSTBP#1 4
Group 2
GTL_D#[47..32] 4
GTL_DINV#2 4
GTL_DSTBN#2 4
GTL_DSTBP#2 4
Group 3
GTL_D#[63..48] 4
GTL_DINV#3 4
GTL_DSTBN#3 4
GTL_DSTBP#3 4
U27A
1/6
AGTL+ I/F
CPU
ADDR. GROUP 0
ADDR. GROUP 1
CONTROL
MISC.
DATA GROUP 0
DATA GROUP 1
DATA GROUP 2
DATA GROUP 3
SC
SB
R882 DUMMY-27KR3
R883 DUMMY-330KR3
D55 DUMMY-BAT54-U1
D56 DUMMY-BAT54-U1
PM_SUS_STAT#
PM_SUS_STAT_IN#
A_RST#
15,33 PM_SUS_STAT#_KBC
Q27 2N7002
R326 10KR3
R328 2K2R3
R327 5K6R3
R232 49D9R2F
R233 100R2F
C279 SC1U16V3KX
R884 0R3-0-U
R289 33R2
NB_PWROK
R248 49D9R3F
R234 24D9R3F
R189 412R2F
C280 SC220P
C231 SC1U10V3KX
TP51 TPAD30
TP52 TPAD30
NB_GTLREF
VCC_CORE
1D8V_S0
2D5V_S3
3D3V_S3
U27C
3/6
MEM I/F
RC300M
M_DATA_R[0..63] 11,12
M_A[15..0] 11
M_SDM_R[7..0] 11,12
M_DQS_R[7..0] 11,12
M_RAS# 11
M_CAS# 11
M_WE# 11
CLK_DDR0# 11
CLK_DDR0 11
CLK_DDR1# 11
CLK_DDR1 11
CLK_DDR2# 11
CLK_DDR2 11
CLK_DDR3# 11
CLK_DDR3 11
CLK_DDR4# 11
CLK_DDR4 11
CLK_DDR5# 11
CLK_DDR5 11
M_CKE0_R# 11,12
M_CKE1_R# 11,12
M_CKE2_R# 11,12
M_CKE3_R# 11,12
M_CS0_R# 11,12
M_CS1_R# 11,12
M_CS2_R# 11,12
M_CS3_R# 11,12
DDR_VREF_S3
C310 SCD47U16V
C348 SCD47U16V
R330 49D9R2F
R329 DUMMY-0R3-0-U
C339 SCD01U6_V
C285 SC1U16V3KX
VCORE_PWROK 17,39
DELAY 15ms
U83C TSLCX14-U
U83D TSLCX14-U
U83E TSLCX14-U
U83F TSLCX14-U
R774 15KR3
C662 SC1U16V3KX
R781 10KR3
R191 DUMMY-4K7R2
R190 10R2
RESISTOR
RC300M MODE
R1
TEST MODE
R2
NORMAL MODE
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Title
ATI RC300M (2/3)
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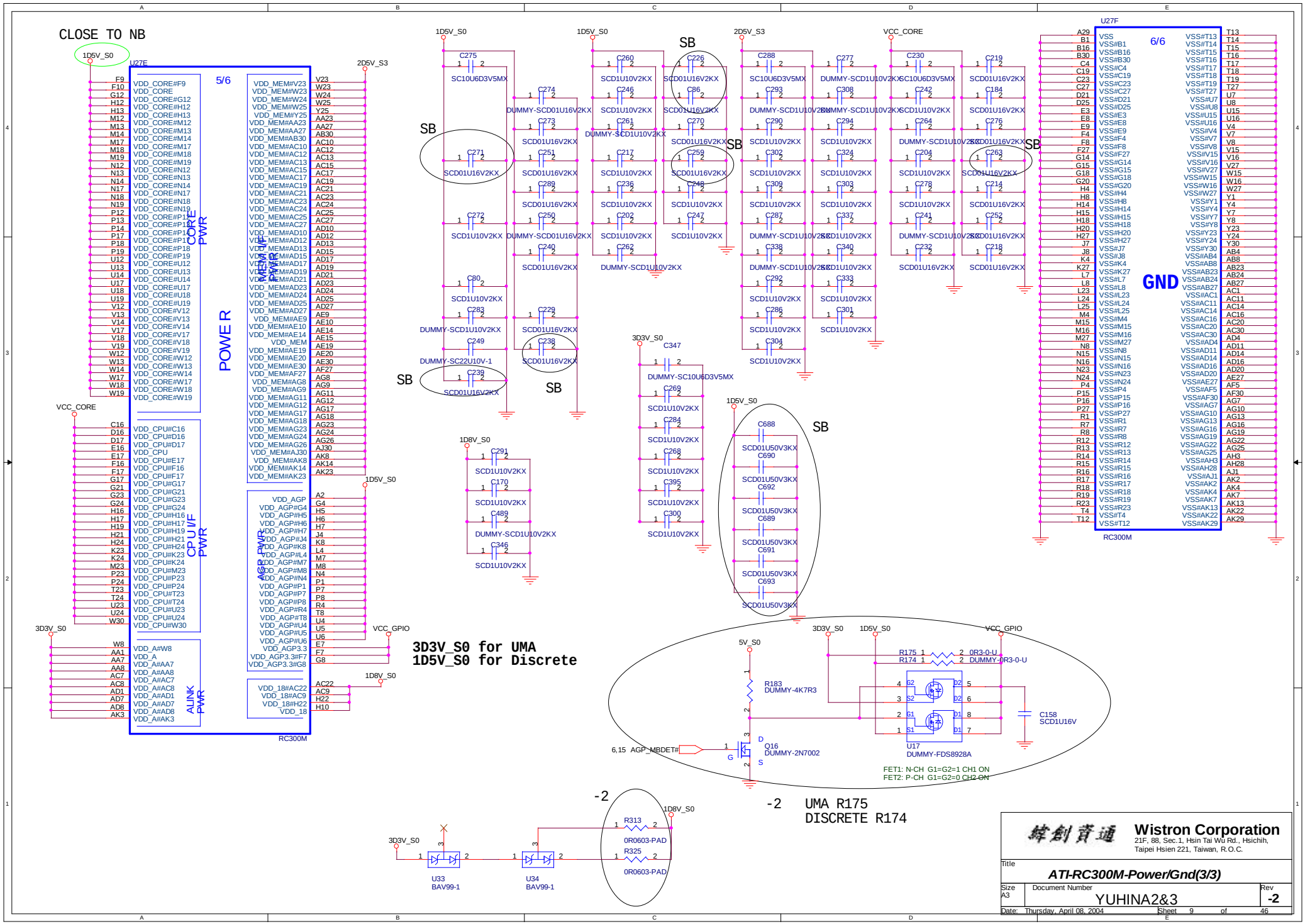
CLOSE TO NB
U27E
5/6
POWER
CORE PWR
CPU I/F PWR
AGP PWR
ALINK PWR
MEM I/O PWR
RC300M
3D3V_S0 for UMA
1D5V_S0 for Discrete
U27F
6/6
GND
RC300M
SB
DUMMY-SCD1U16V2KX
DUMMY-SC22U10V-1
DUMMY-SC10U6D3V5MX
SCD1U10V2KX
SCD1U16V2KX
SCD1U50V3KX
R183 DUMMY-4K7R3
Q16 DUMMY-2N7002
U17 DUMMY-FDS8928A
R175 0R3-0-U
R174 DUMMY-0R3-0-U
C158 SCD1U16V
FET1: N-CH G1=G2=1 CH1 ON
FET2: P-CH G1=G2=0 CH2 ON
-2 UMA R175
DISCRETE R174
R313 0R0603-PAD
R325 0R0603-PAD
U33 BAV99-1
U34 BAV99-1
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Title
ATI-RC300M-Power/Gnd(3/3)
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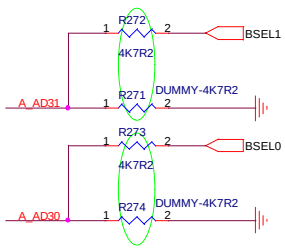
RC300M STRAPPING



A_AD[31..30] : FSB CLK SPEED
Default: 00
00: 100MHZ
01: 133MHZ
10: 200MHZ
11: 166MHZ

A_AD29 : STRAP CONFIGURATION
Default : 1
0: REDUCEDE SET
1: FULL SET

A_AD28 :SPREAD SPECTRUM ENABLE
Default : 0
0: DISABLE SS
1: ENABLE SS

A_AD27 :FrcShortTReset#
Default : 1
0: TESTE MODE
1: NORMAL MODE

A_AD26 :ENABLE IOQ
Default : 1
0: IOQ=1
1: IOQ=12

A_AD25,A_AD17 :CPU VOLTAGE[1..0]
Default : 01
00: 1.05V (MOBILE CPU)
01: 1.35V (MOBILE CPU)
10: 1.45V (DESKTOP CPU)
11: 1.75V (DESKTOP CPU)

A_AD24 :MOBILE CPU SELECT
Default : 1
0: BANIAS CPU
1: NOT BANIAS CPU

A_AD23 :CLOCK BYPASS DISABLE
Default : 1
0: TEST MODE
1: NORMAL OPERATION

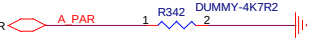
A_AD22 :OSC PAD OUTPUT PCICLK
Default : 1
0: OSC PIN DRIVES PCICLK
1: OSC PIN DRIVES OSC CLK

A_AD21 :AUTO_CAL ENABLE
Default : 1
0: DISABLE AUTO_CAL
1: ENABLE AUTO_CAL

A_AD20 :INTERNAL CLK GEN ENABLE
Default : 1
0: EXTERNAL CLOCK GENERATOR
1: INTERNAL CLOCK GENERATOR

A_AD19 :MEMORY IO VOLTAGE SELECTION
Default : 1
0: 1.8V
1: 2.5V

A_AD18 :ENABLE PHASE CALIBRATION
Default : 0
0: DISABLE
1: ENABLE



PAR :EXTENDED DEBUG MODE
Default : 1
0: DEBUG MODE
1: NORMAL OPERATION

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Title: **NB_STRAPPING**

Size: A3 | Document Number: **YUHINA2&3** | Rev: **-2**

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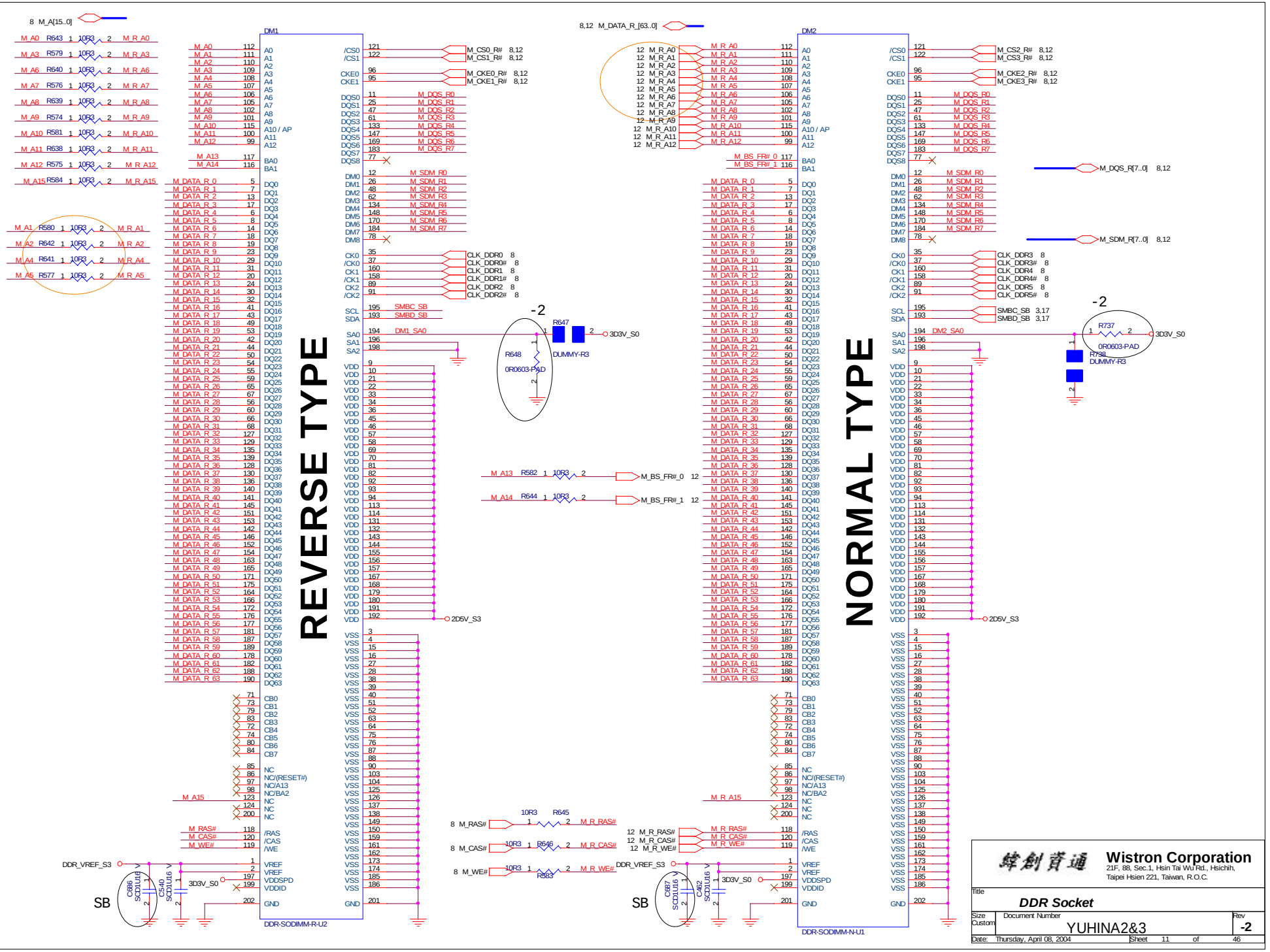
REVERSE TYPE
NORMAL TYPE
DM1
DM2
DDR-SODIMM-R-U2
DDR-SODIMM-N-U1
8 M_A[15..0]
8,12 M_DATA_R_[63..0]
M_A0 R643 10R3 M_R_A0
M_A3 R579 10R3 M_R_A3
M_A6 R640 10R3 M_R_A6
M_A7 R576 10R3 M_R_A7
M_A8 R639 10R3 M_R_A8
M_A9 R574 10R3 M_R_A9
M_A10 R581 10R3 M_R_A10
M_A11 R638 10R3 M_R_A11
M_A12 R575 10R3 M_R_A12
M_A15 R584 10R3 M_R_A15
M_A1 R580 10R3 M_R_A1
M_A2 R642 10R3 M_R_A2
M_A4 R641 10R3 M_R_A4
M_A5 R577 10R3 M_R_A5
M_CS0_R# 8,12
M_CS1_R# 8,12
M_CKE0_R# 8,12
M_CKE1_R# 8,12
M_CS2_R# 8,12
M_CS3_R# 8,12
M_CKE2_R# 8,12
M_CKE3_R# 8,12
M_DQS_R[7..0] 8,12
M_SDM_R[7..0] 8,12
CLK_DDR0 8
CLK_DDR0# 8
CLK_DDR1 8
CLK_DDR1# 8
CLK_DDR2 8
CLK_DDR2# 8
CLK_DDR3 8
CLK_DDR3# 8
CLK_DDR4 8
CLK_DDR4# 8
CLK_DDR5 8
CLK_DDR5# 8
SMBC_SB 3,17
SMBD_SB 3,17
-2
R647
R648 0R0603-PAD
DUMMY-R3
R737 0R0603-PAD
R738 DUMMY-R3
DM1_SA0
DM2_SA0
3D3V_S0
2D5V_S3
M_A13 R582 10R3 M_BS_FR#_0 12
M_A14 R644 10R3 M_BS_FR#_1 12
M_RAS# R645 10R3
M_CAS# R646 10R3
M_WE# R583 10R3
DDR_VREF_S3
SB
C686 SCD1U16V
C540 SCD1U16V
C687 SCD1U16V
C462 SCD1U16V
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PARALLEL TERMINATION

PULL HIGH STUBS < 0.8", PLACE RPs CLOSE TO DM2
NO EQUAL LENGTH LIMITATION

M_DATA_R_[63..0] 8,11
M_DQS_R[7..0] 8,11
M_SDM_R[7..0] 8,11

1D25V_S0 2D5V_S3

RN46: M_DATA_R_6 M_SDM_R0 M_DATA_R_4 M_DATA_R_5 — SRN56 — C619 SCD1U16V; C603 SCD1U16V
RN47: M_SDM_R1 M_DATA_R_13 M_DATA_R_12 M_DATA_R_7 — SRN56 — C620 DUMMY-SCD1U16V
RN28: M_DATA_R_2 M_DQS_R0 M_DATA_R_1 M_DATA_R_0 — SRN56 — C570 SCD1U16V; C559 SCD1U16V
RN29: M_DQS_R1 M_DATA_R_9 M_DATA_R_8 M_DATA_R_3 — SRN56 — C571 DUMMY-SCD1U16V
RN31: M_DATA_R_24 M_DATA_R_19 M_DATA_R_18 M_DQS_R2 — SRN56 — C561 SCD1U16V; C573 SCD1U16V
RN32: M_DATA_R_27 M_DATA_R_26 M_DQS_R3 M_DATA_R_25 — SRN56 — C574 DUMMY-SCD1U16V
RN48: M_DATA_R_20 M_DATA_R_21 M_DATA_R_15 M_DATA_R_14 — SRN56 — C621 SCD1U16V; C604 SCD1U16V
RN30: M_DATA_R_16 M_DATA_R_17 M_DATA_R_11 M_DATA_R_10 — SRN56 — C572 DUMMY-SCD1U16V
RN49: M_DATA_R_28 M_DATA_R_23 M_DATA_R_22 M_SDM_R2 — SRN56 — C623 SCD1U16V; C624 SCD1U16V
RN50: M_DATA_R_31 M_DATA_R_30 M_SDM_R3 M_DATA_R_29 — SRN56 — C605 DUMMY-SCD1U16V
RN56: M_DATA_R_53 M_DATA_R_52 M_DATA_R_46 M_DATA_R_47 — SRN56 — C562 SCD1U16V; C586 SCD1U16V
RN37: M_DATA_R_49 M_DATA_R_48 M_DATA_R_43 M_DATA_R_42 — SRN56 — C636 DUMMY-SCD1U16V
RN54: M_DATA_R_38 M_SDM_R4 M_DATA_R_37 M_DATA_R_36 — SRN56 — C633 SCD1U16V; C634 SCD1U16V
RN55: M_SDM_R5 M_DATA_R_45 M_DATA_R_44 M_DATA_R_39 — SRN56 — C635 DUMMY-SCD1U16V
RN35: M_DATA_R_34 M_DQS_R4 M_DATA_R_33 M_DATA_R_32 — SRN56 — C583 SCD1U16V; C585 SCD1U16V
RN36: M_DATA_R_41 M_DQS_R5 M_DATA_R_40 M_DATA_R_35 — SRN56 — C584 DUMMY-SCD1U16V
RN57: M_DATA_R_60 M_DATA_R_55 M_DATA_R_54 M_SDM_R6 — SRN56 — C637 SCD1U16V; C638 SCD1U16V
RN58: M_DATA_R_63 M_DATA_R_62 M_SDM_R7 M_DATA_R_61 — SRN56 — C639 DUMMY-SCD1U16V
RN38: M_DATA_R_56 M_DATA_R_50 M_DATA_R_51 M_DQS_R6 — SRN56 — C589 SCD1U16V; C587 SCD1U16V
RN39: M_DATA_R_59 M_DATA_R_58 M_DQS_R7 M_DATA_R_57 — SRN56 — C588 DUMMY-SCD1U16V

CPC Address

1D25V_S0 2D5V_S3

RN34: 11 M_R_WE# 8,11 M_CS2_R# 11 M_BS_FR#_0 8,11 M_CS0_R# — SRN33 — C581 SCD1U16V; C582 SCD1U16V
RN52: 11 M_R_A0 8,11 M_CS1_R# 11 M_R_A2 — M_R_A0 — SRN33 — C629 SCD1U16V; C632 SCD1U16V

Address / Command

1D25V_S0

RN51: 11 M_R_A4 11 M_R_A6 — M_R_A6; 11 M_R_A8 — M_R_A8 — SRN33 — C627 SCD1U16V; C626 SCD1U16V
RN53: 8,11 M_CS3_R# 11 M_R_CAS# 11 M_BS_FR#_1 11 M_R_RAS# — SRN33 — C630 SCD1U16V; C631 SCD1U16V
11 M_R_A3 — M_R_A3 33R2 — R684; 11 M_R_A12 — M_R_A12 33R2 — R682; 11 M_R_A11 — M_R_A11 33R2 — R736 — C576 SCD1U16V; C580 SCD1U16V
RN33: 11 M_R_A10 11 M_R_A1 11 M_R_A5 — M_R_A10 — SRN33 — C578 SCD1U16V; C579 SCD1U16V

Control

1D25V_S0 2D5V_S3

8,11 M_CKE2_R# — 33R2 R735; 8,11 M_CKE3_R# — 33R2 R680
8,11 M_CKE1_R# 8,11 M_CKE0_R# — 33R2 R573; 33R2 R637
11 M_R_A7 11 M_R_A9 — M_R_A7 33R2 — R683; M_R_A9 33R2 — R681 — C577 SCD1U16V; C575 SCD1U16V
C625 SCD1U16V; C628 SCD1U16V; C622 SCD1U16V; C468 SCD1U16V

PLACE CAPS BETWEEN AND NEAR DDR SKTS
PLACE EACH 0.1UF CAP CLOSE TO POWER PIN

2D5V_S3

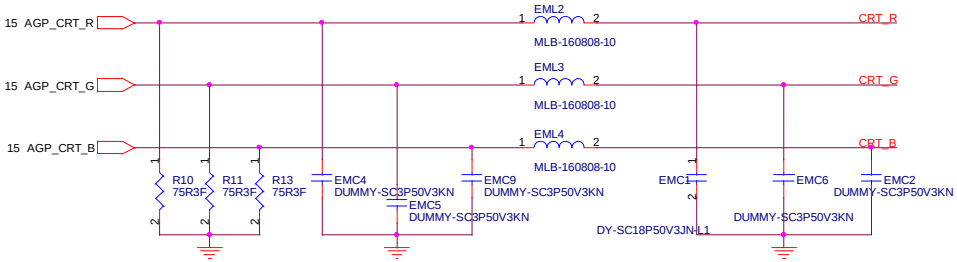
C607 C524 C469 C467 C464 C463 C470 C520 — SCD1U16V
C525 C466 C465 C519 C523 C606 C471 C560 — SCD1U16V
C522 SCD1U16V DUMMY-SC10U6D3V5MX; C515 SC10U6D3V5MX; C518 SC10U6D3V5MX; C608 C609 C526 C521 — SCD1U16V

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR Serial/Terminator Resistor
Size: A3 | Document Number: YUHINA2&3 | Rev: -2
Date: Thursday, April 08, 2004 | Sheet 12 of 46

CRT I/F & CONNECTOR

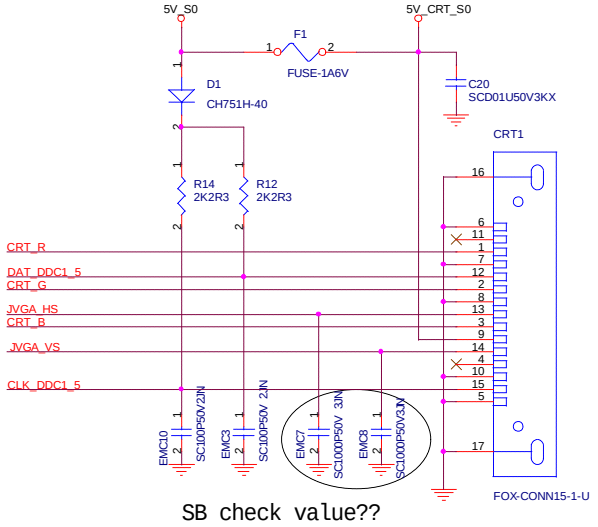
Ferrite bead impedance: 75ohm@100MHz



Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
**** 37.4_1% resistors must be placed at the same place as the RGB 75 Ohm pull-down resistors.***

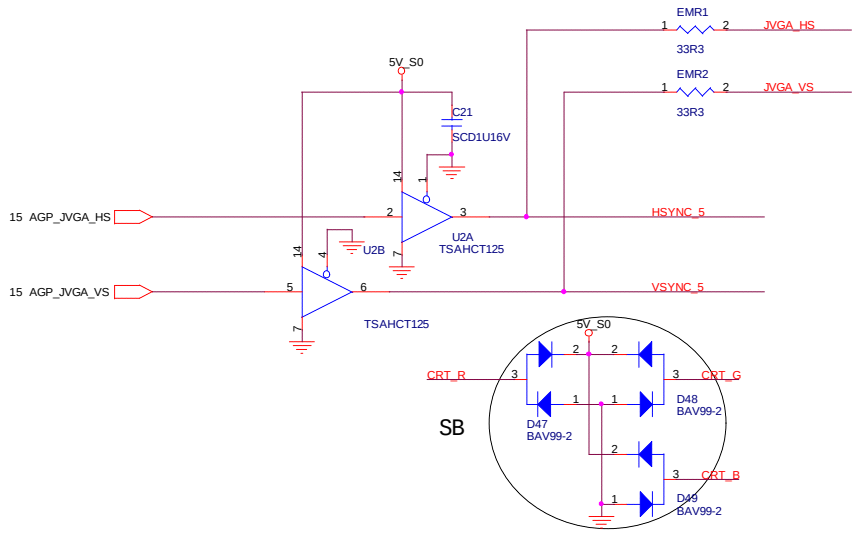
Pi-filter & 75 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

RDDP 1.0

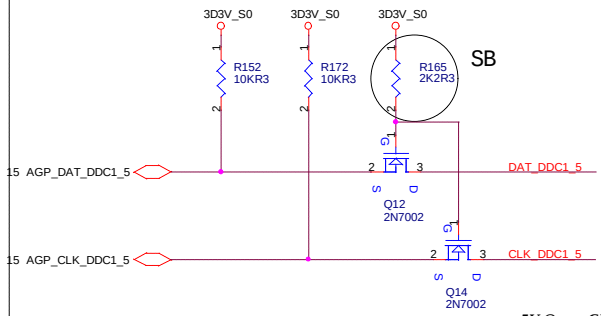


SB check value??

Hsync & Vsync level shift



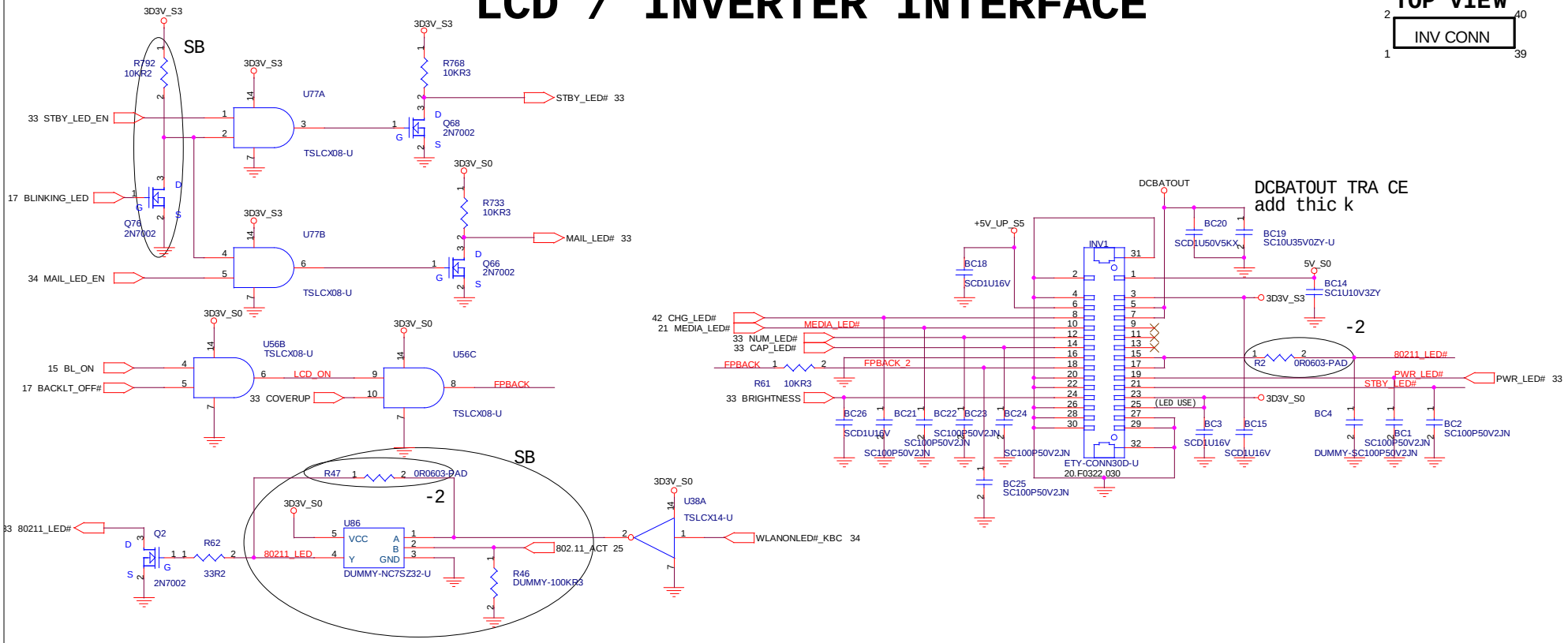
DDC_CLK & DATA level shift

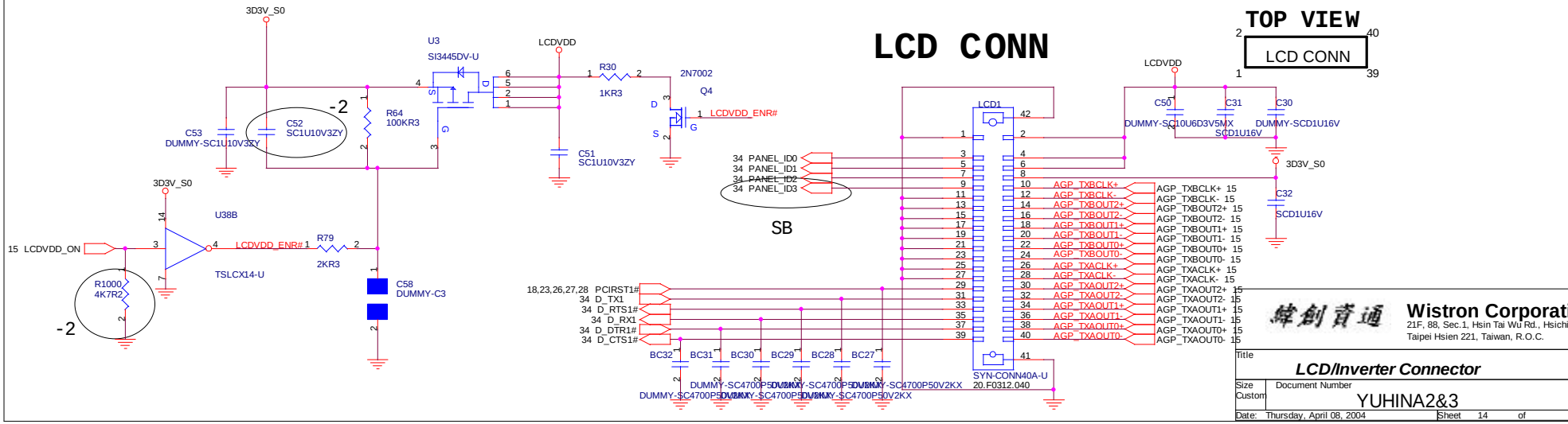


5V @ ext. CRT side

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ***CRT Connector***		
Size: A3	Document Number: YUHINA2&3	Rev: -2
Date: Thursday, April 08, 2004	Sheet 13 of 46	

LCD / INVERTER INTERFACE





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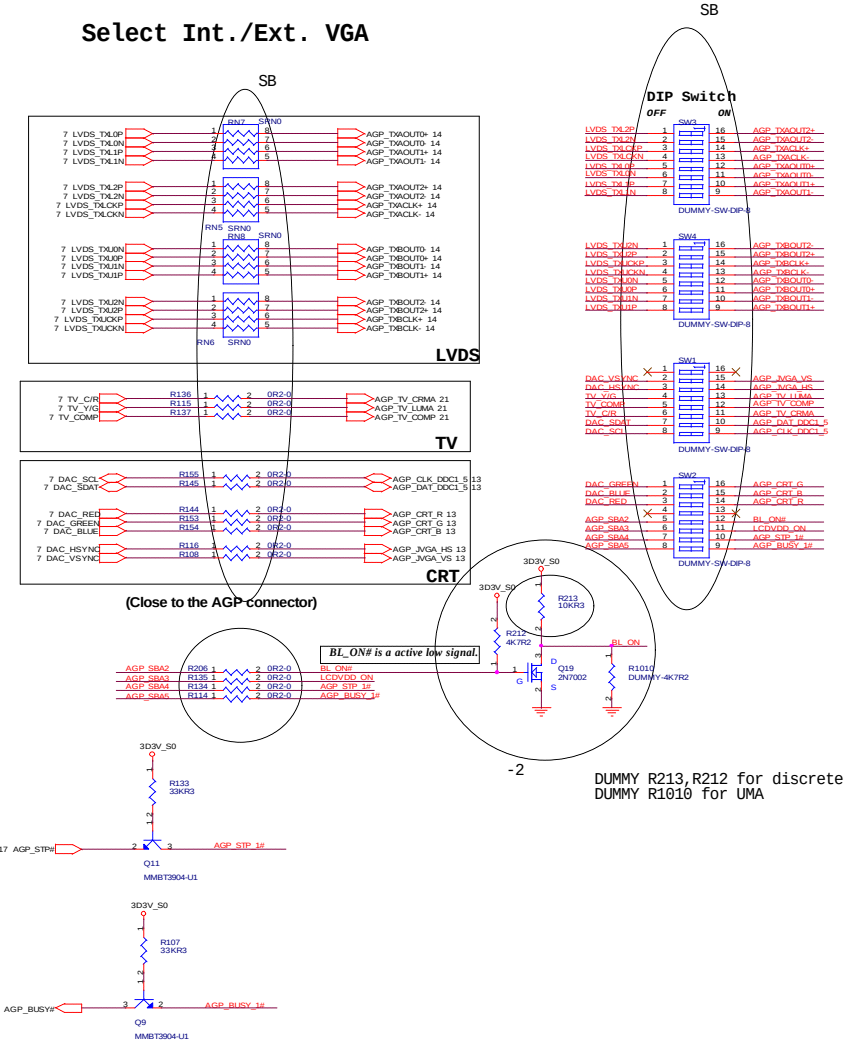
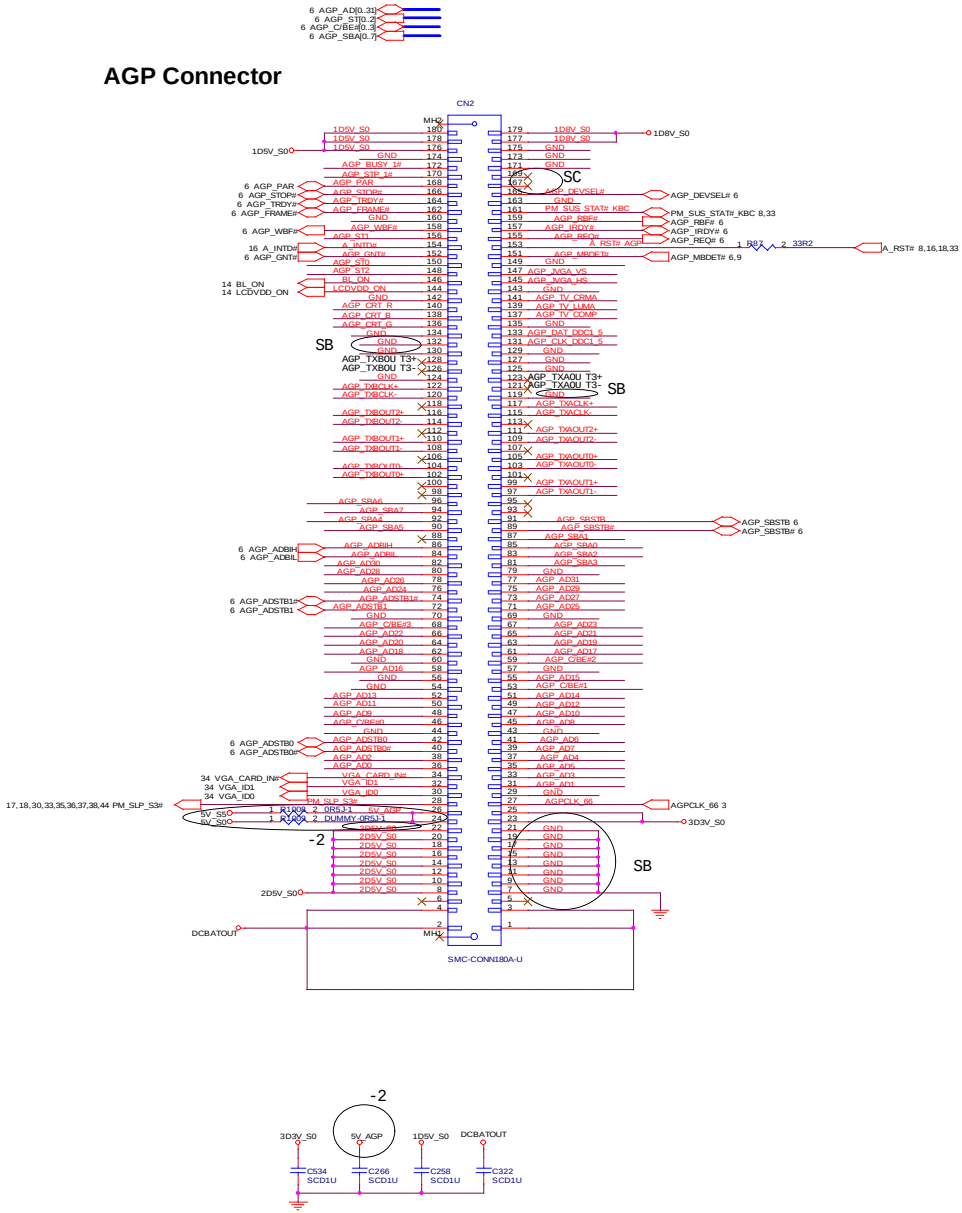
Title	***LCD/Inverter Connector***	
Size: Custom	Document Number: YUHINA2&3	Rev: -2
Date: Thursday, April 08, 2004	Sheet 14 of 46	

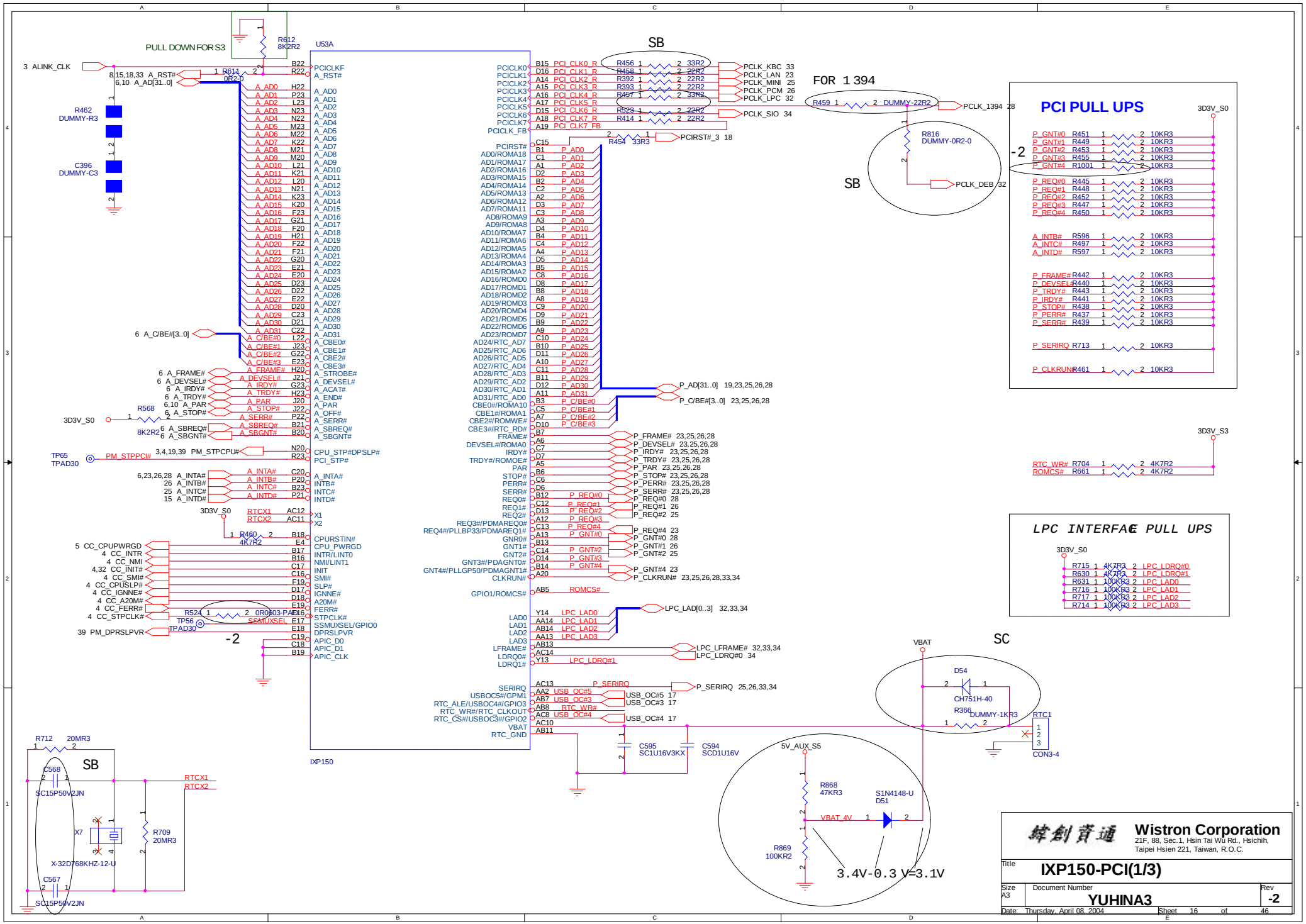
Select Int./Ext. VGA

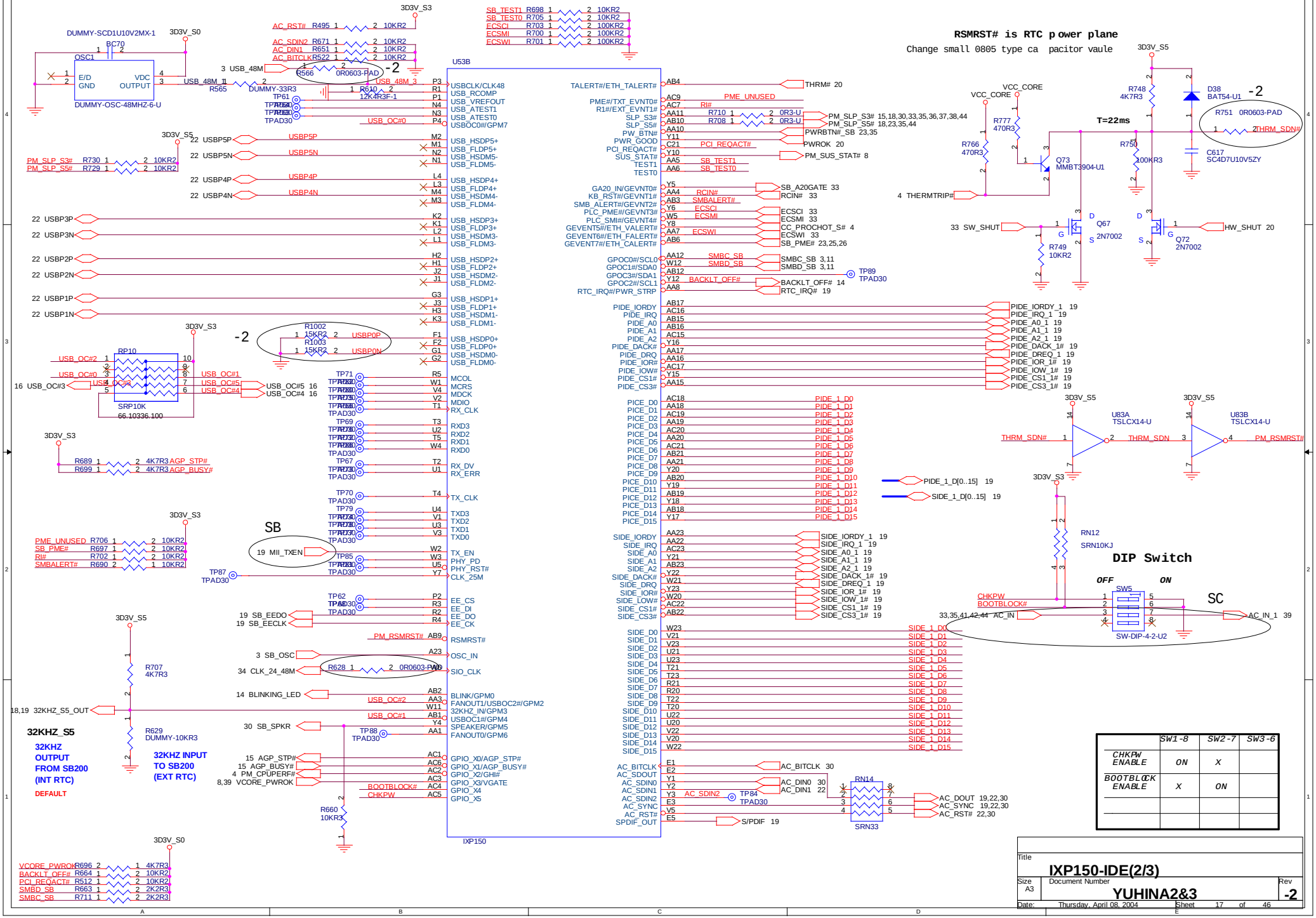


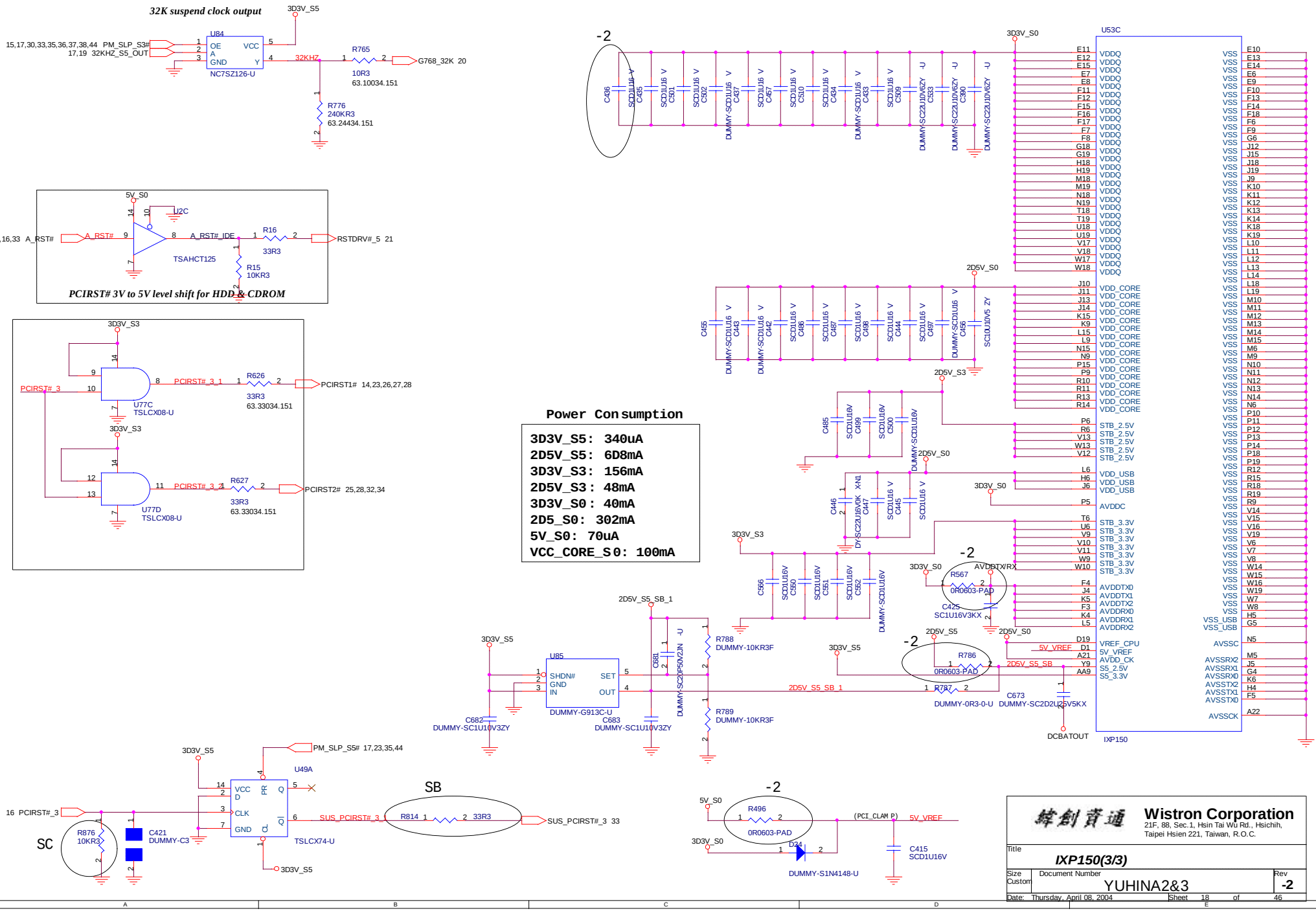
AGP Connector

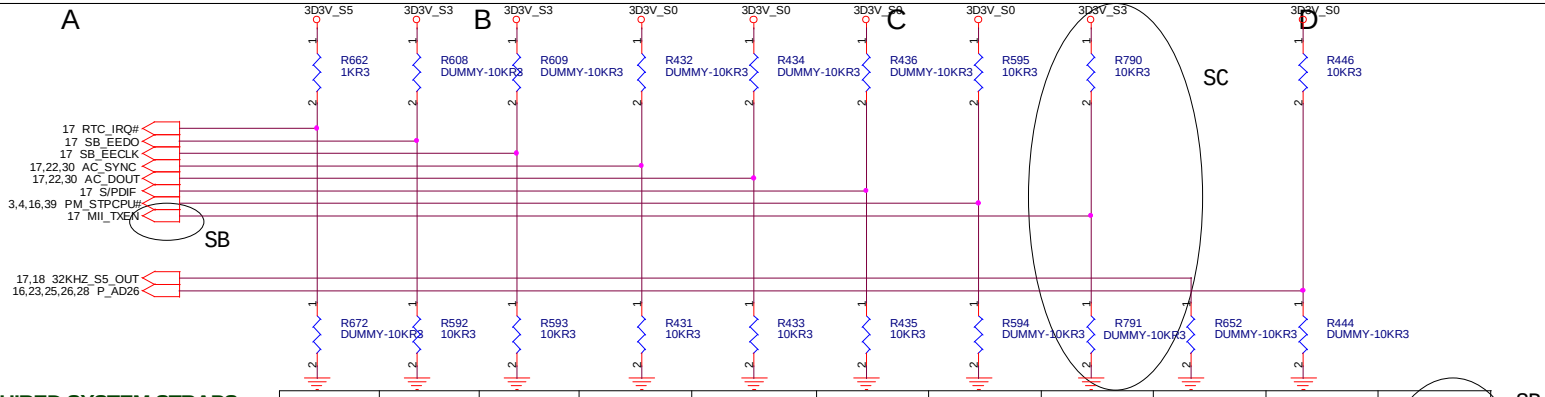


Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title: AGP Connector			
Size: A2	Document Number: YUHINA2&3	Rev: -2	
Date: Thursday, April 08, 2004	Sheet 15 of 46		


PULL DOWN FOR S3
R612 8K2R2
U53A
IXP150
SB
FOR 1 394
R459 DUMMY-22R2
PCLK_1394 28
R816 DUMMY-0R2-0
PCLK_DEB 32
PCI PULL UPS
3D3V_S0
P_GNT#0 R451 10KR3
P_GNT#1 R449 10KR3
P_GNT#2 R453 10KR3
P_GNT#3 R455 10KR3
P_GNT#4 R1001 10KR3
P_REQ#0 R445 10KR3
P_REQ#1 R448 10KR3
P_REQ#2 R452 10KR3
P_REQ#3 R447 10KR3
P_REQ#4 R450 10KR3
A_INTB# R596 10KR3
A_INTC# R497 10KR3
A_INTD# R597 10KR3
P_FRAME# R442 10KR3
P_DEVSEL# R440 10KR3
P_TRDY# R443 10KR3
P_IRDY# R441 10KR3
P_STOP# R438 10KR3
P_PERR# R437 10KR3
P_SERR# R439 10KR3
P_SERIRQ R713 10KR3
P_CLKRUN# R461 10KR3
3D3V_S3
RTC_WR# R704 4K7R2
ROMCS# R661 4K7R2
LPC INTERFACE PULL UPS
3D3V_S0
R715 4K7R3 LPC_LDRQ#0
R630 4K7R3 LPC_LDRQ#1
R631 100KR3 LPC_LAD0
R716 100KR3 LPC_LAD1
R717 100KR3 LPC_LAD2
R714 100KR3 LPC_LAD3
SC
VBAT
D54 CH751H-40
R366 DUMMY-1KR3
RTC1 CON3-4
5V_AUX_S5
R868 47KR3
S1N4148-U D51
VBAT_4V
R869 100KR2
3.4V-0.3 V=3.1V
C595 SC1U16V3KX
C594 SCD1U16V
R712 20MR3
C568 SC15P50V2JN
X7 X-32D768KHZ-12-U
R709 20MR3
C567 SC15P50V2JN
R462 DUMMY-R3
C396 DUMMY-C3
R568 8K2R2
TP65 TPAD30
R524 0R0303-PAD
TP56 TPAD30
R611 0R2-0
R460 4K7R2
-2
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
IXP150-PCI(1/3)
Size A3
Document Number
YUHINA3
Rev -2
Date: Thursday, April 08, 2004
Sheet 16 of 46


RSMRST# is RTC p ower plane
Change small 0805 type ca pacitor vaule
U53B
IXP150
DUMMY-SCD1U10V2MX-1
DUMMY-OSC-48MHZ-6-U
DUMMY-33R3
DUMMY-10KR3
SRP10K
66.10336.100
SB
32KHZ_S5
32KHZ OUTPUT FROM SB200 (INT RTC)
DEFAULT
32KHZ INPUT TO SB200 (EXT RTC)
T=22ms
DIP Switch
OFF
ON
SW-DIP-4-2-U2
SRN10KJ
SRN33
TSLCX14-U
Q73 MMBT3904-U1
Q67 2N7002
Q72 2N7002
BAT54-U1
C617 SC4D7U10V5ZY
SW1-8
SW2-7
SW3-6
CHKPW ENABLE
BOOTBLOCK ENABLE
Title
IXP150-IDE(2/3)
Size A3
Document Number
YUHINA2&3
Rev -2
Date: Thursday, April 08, 2004
Sheet 17 of 46


32K suspend clock output
3D3V_S5
U84
15,17,30,33,35,36,37,38,44 PM_SLP_S3#
17,19 32KHZ_S5_OUT
OE
A
GND
VCC
Y
NC7SZ126-U
32KHZ
R765
10R3
63.10034.151
G768_32K 20
R776
240KR3
63.24434.151
5V_S0
U2C
8,15,16,33 A_RST#
A_RST#
A_RST#_IDE
TSAHCT125
R16
33R3
R15
10KR3
RSTDRV#_5 21
PCIRST# 3V to 5V level shift for HDD & CDROM
3D3V_S3
PCIRST#_3
PCIRST#_3_1
R626
33R3
63.33034.151
PCIRST1# 14,23,26,27,28
U77C
TSLCX08-U
PCIRST#_3_2
R627
PCIRST2# 25,28,32,34
U77D
Power Consumption
3D3V_S5: 340uA
2D5V_S5: 6D8mA
3D3V_S3: 156mA
2D5V_S3: 48mA
3D3V_S0: 40mA
2D5_S0: 302mA
5V_S0: 70uA
VCC_CORE_S0: 100mA
U53C
IXP150
3D3V_S0
2D5V_S0
2D5V_S3
2D5V_S5_SB_1
2D5V_S5_SB
U85
SHDN#
GND
IN
SET
OUT
DUMMY-G913C-U
R788
DUMMY-10KR3F
R789
DUMMY-10KR3F
R786
0R0603-PAD
R787
DUMMY-0R3-0-U
C673
DUMMY-SC2D2U6V5KX
DCBATOUT
AVDDTX/RX
R567
C425
SC1U16V3KX
5V_VREF
VREF_CPU
AVDD_CK
S5_2.5V
S5_3.3V
SB
SC
U49A
PM_SLP_S5# 17,23,35,44
16 PCIRST#_3
R876
10KR3
C421
DUMMY-C3
SUS_PCIRST#_3_1
R814
33R3
SUS_PCIRST#_3 33
TSLCX74-U
R496
0R0603-PAD
(PCI_CLAM P)
D24
DUMMY-S1N4148-U
C415
SCD1U16V
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
IXP150(3/3)
Size
Custom
Document Number
YUHINA2&3
Rev
-2
Date: Thursday, April 08, 2004
Sheet 18 of 46



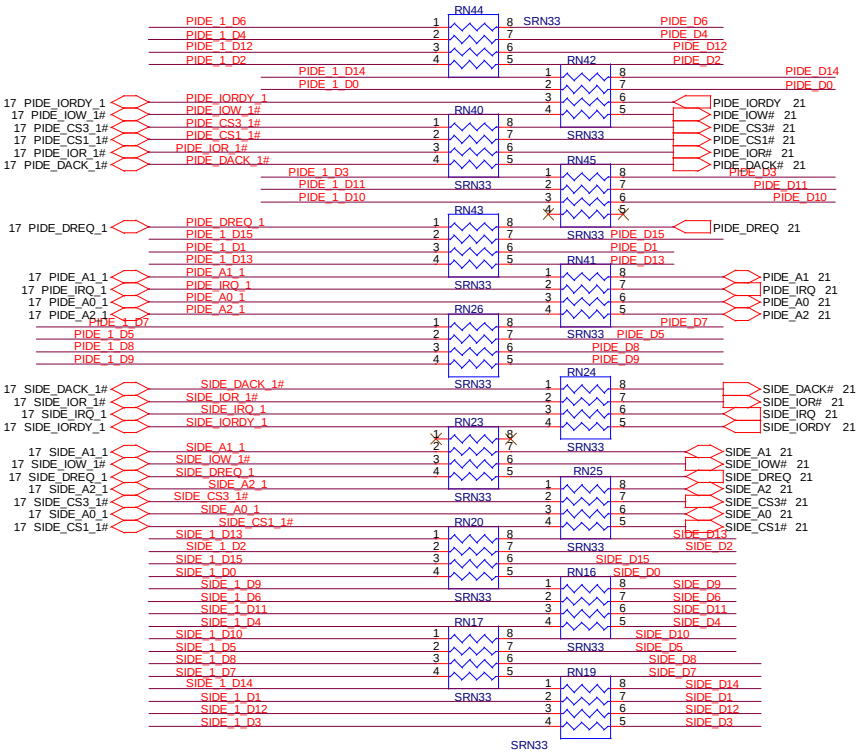
REQUIRED SYSTEM STRAPS

OVERLAP COMMO N PADS
FOR DUAL -OP
RESISTO RS

	ACPWRON	EEDO	EECK	AC_SYNC	AC_SDOUT	SPDIF_OUT	CPU_STP#	32KHZ_S5	PCI_AD26	TX_EN
STRAP HIGH	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS DEFAULT	ROM ON PCI BUS	INIT ACTIVE HIGH(AMD)	33MHz NB BUS	SIO 24MHz	ENABLE SPEED STEP DEFAULT	32KHZ OUTPUT FROM SB200 (INT RTC) DEFAULT	BIOS use LPC cycle DEFAULT	DISABLE CPU FREQ SETTING DEFAULT
STRAP LOW	AUTO PWR ON	IGNORE DEBUG STRAPS	ROM ON LPC BUS DEFAULT	INIT ACTIVE LOW (PIII) DEFAULT	HI SPEED A-LINK DEFAULT	SIO 48MHz DEFAULT	DISABLE SPEED STEP	32KHZ INPUT TO SB200 (EXT RTC)	BIOS uSE FWH Cycle	ENABLE CPU FREQSETTING

SB

PIDE_1_D[0..15] 17
SIDE_1_D[0..15] 17
PIDE_D[0..15] 21
SIDE_D[0..15] 21



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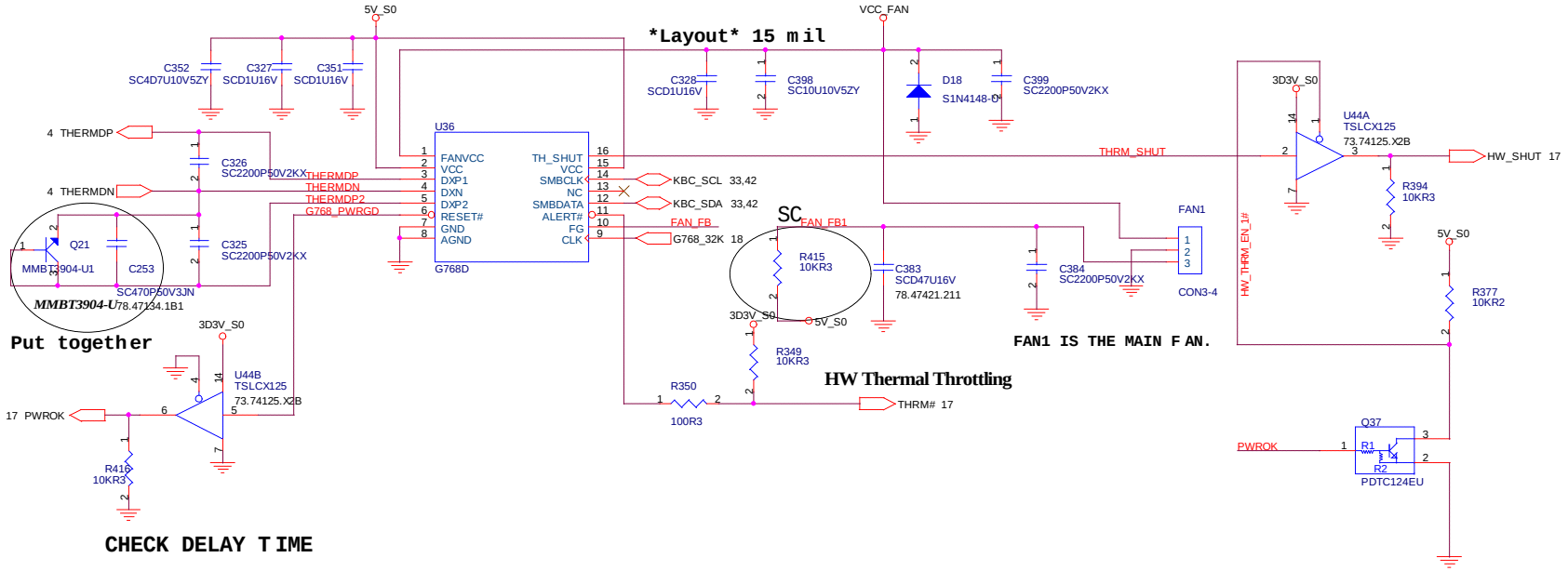
Taipei Hsien 221, Taiwan, R.O.C.

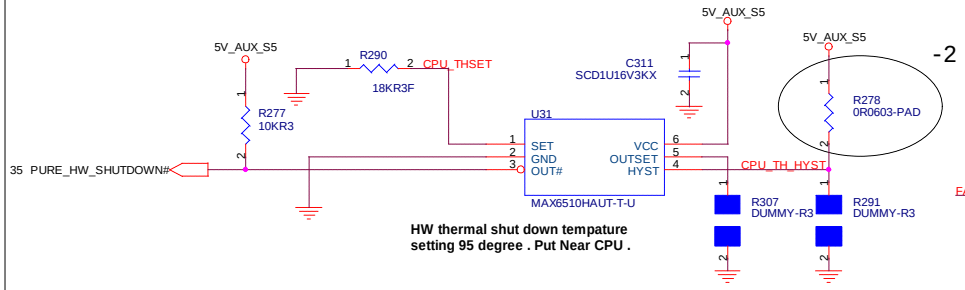
Title: **SB_STRAPPING**

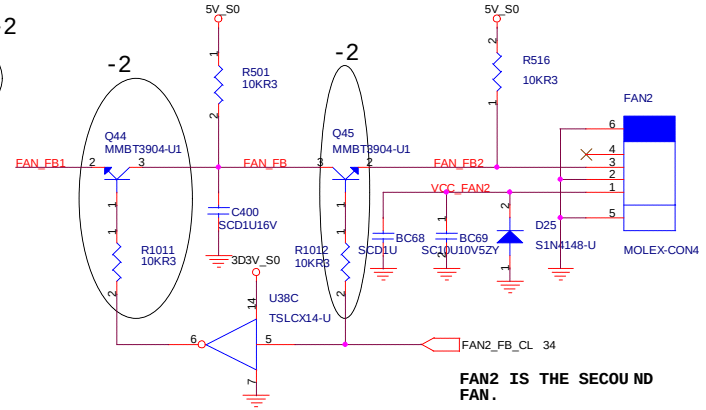
Size: A3 | Document Number: **YUHINA2&3** | Rev: **-2**

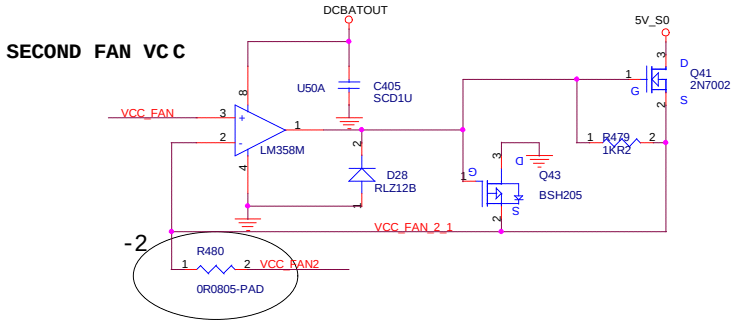
Date: Thursday, April 08, 2004 | Sheet 19 of 46

G768D thermal sensor & Fan controller



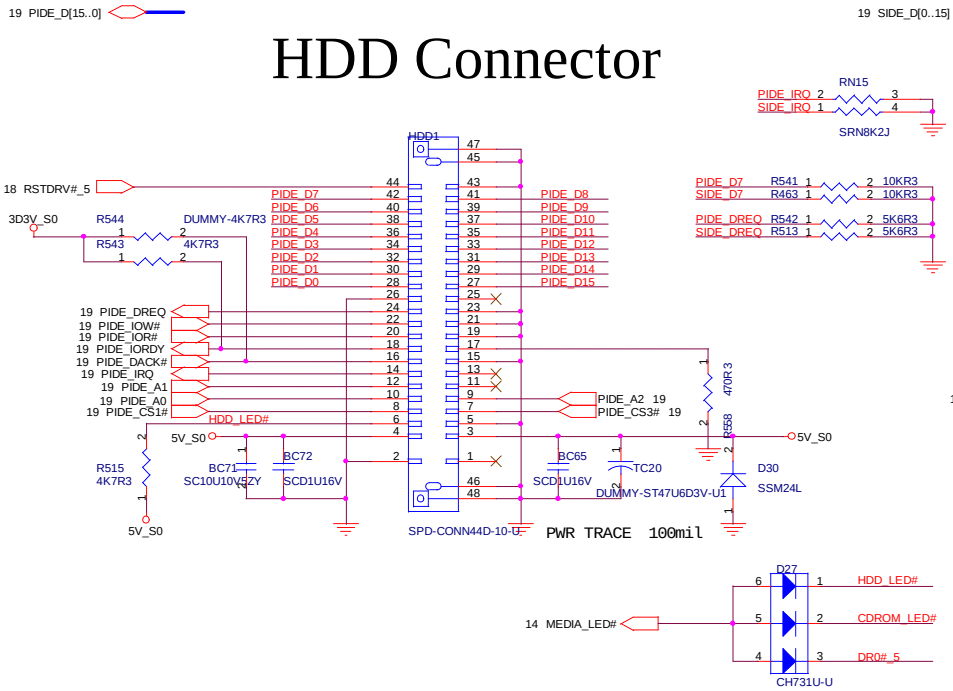




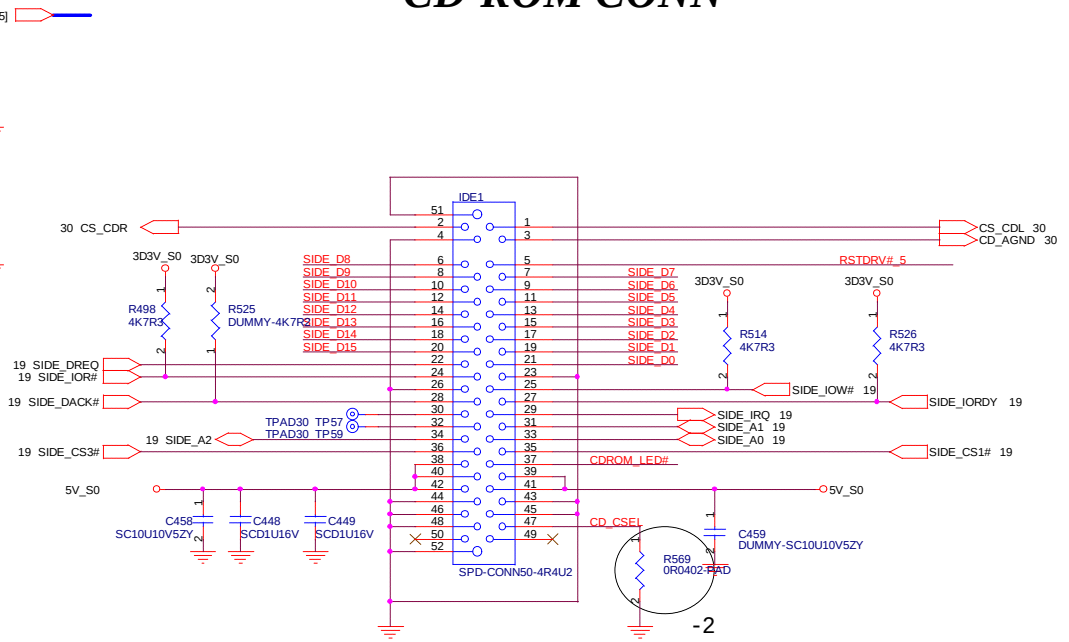


Wistron Corporation 緯創資通		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *Thermal/Fan Controllor*		
Size: Custom	Document Number: YUHINA2&3	Rev: -2
Date: Thursday, April 08, 2004	Sheet 20 of 46	

HDD Connector

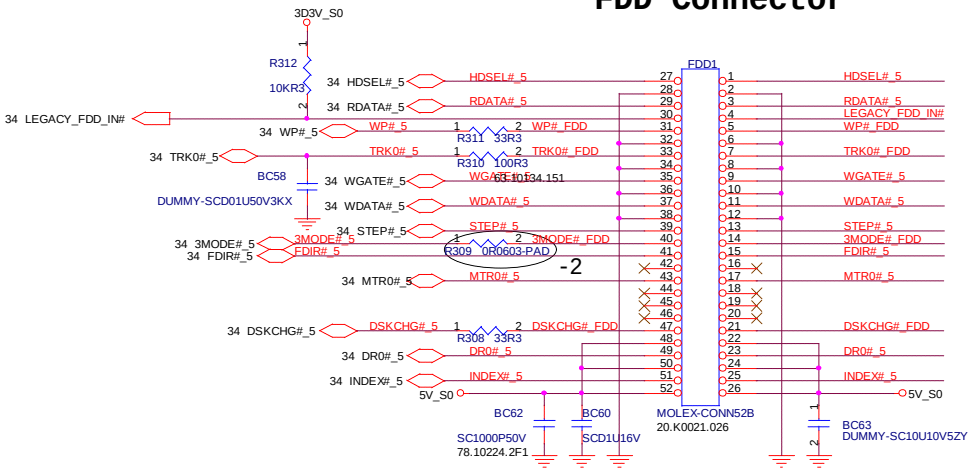


CD-ROM CONN

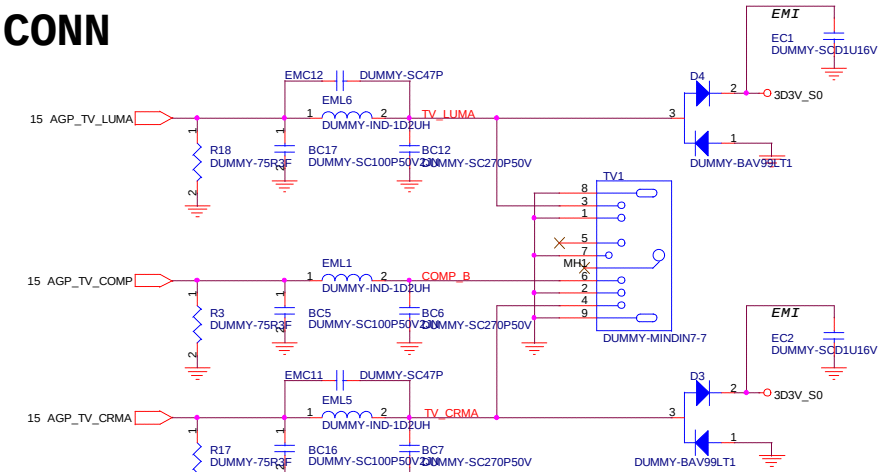


CHECK PIDE/SIDE DIAG# PIN

FDD Connector



TV CONN



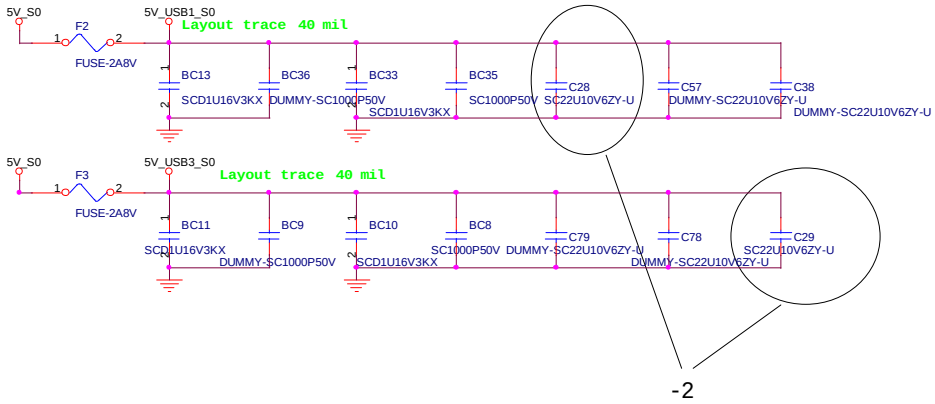
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

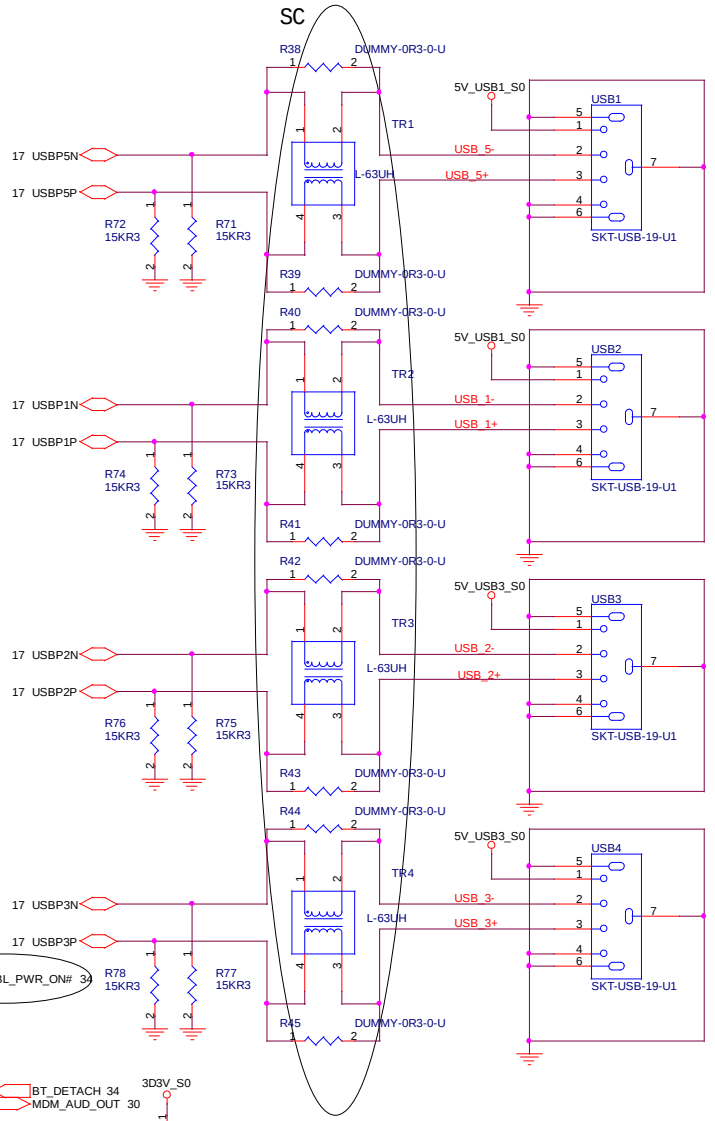
Title: **HDD and CDROM and FDD CONN/TV CONN**

Size	Document Number	Rev
A3	YUHINA2&3	-2

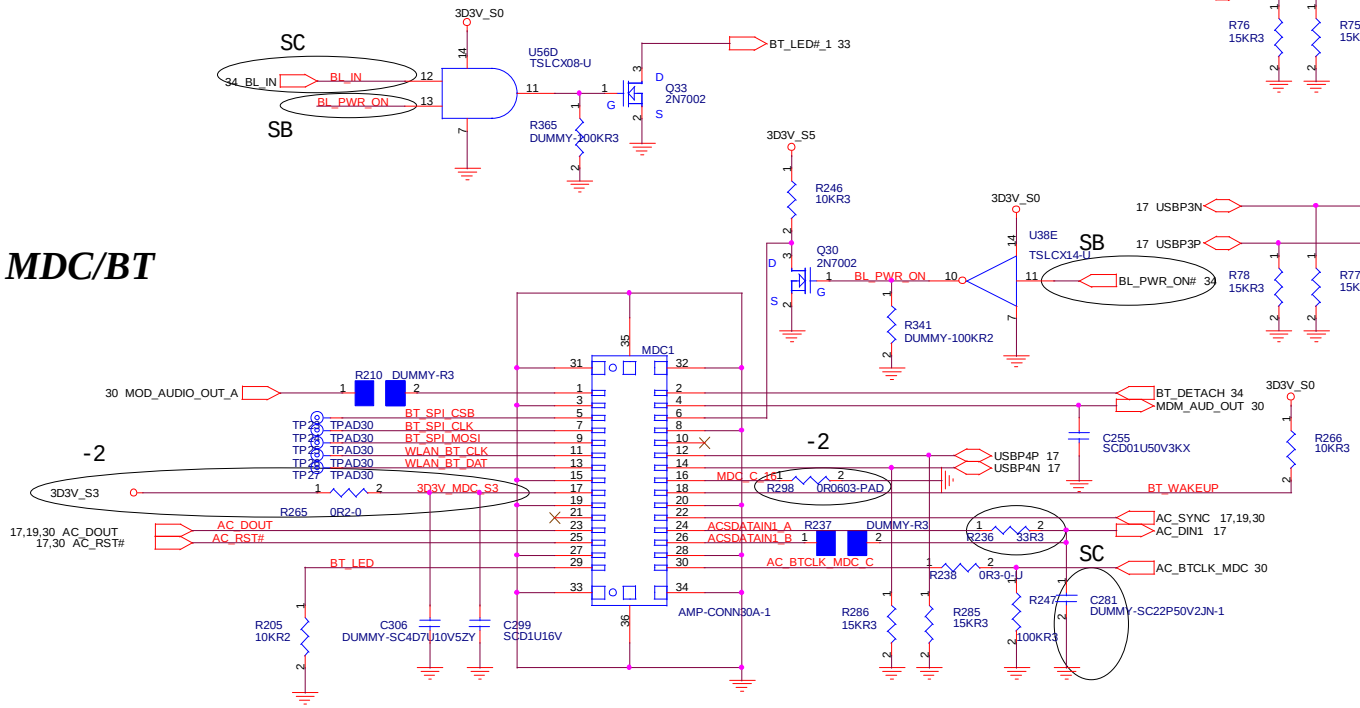
Date: Thursday, April 08, 2004 Sheet 21 of 46

USB PORT

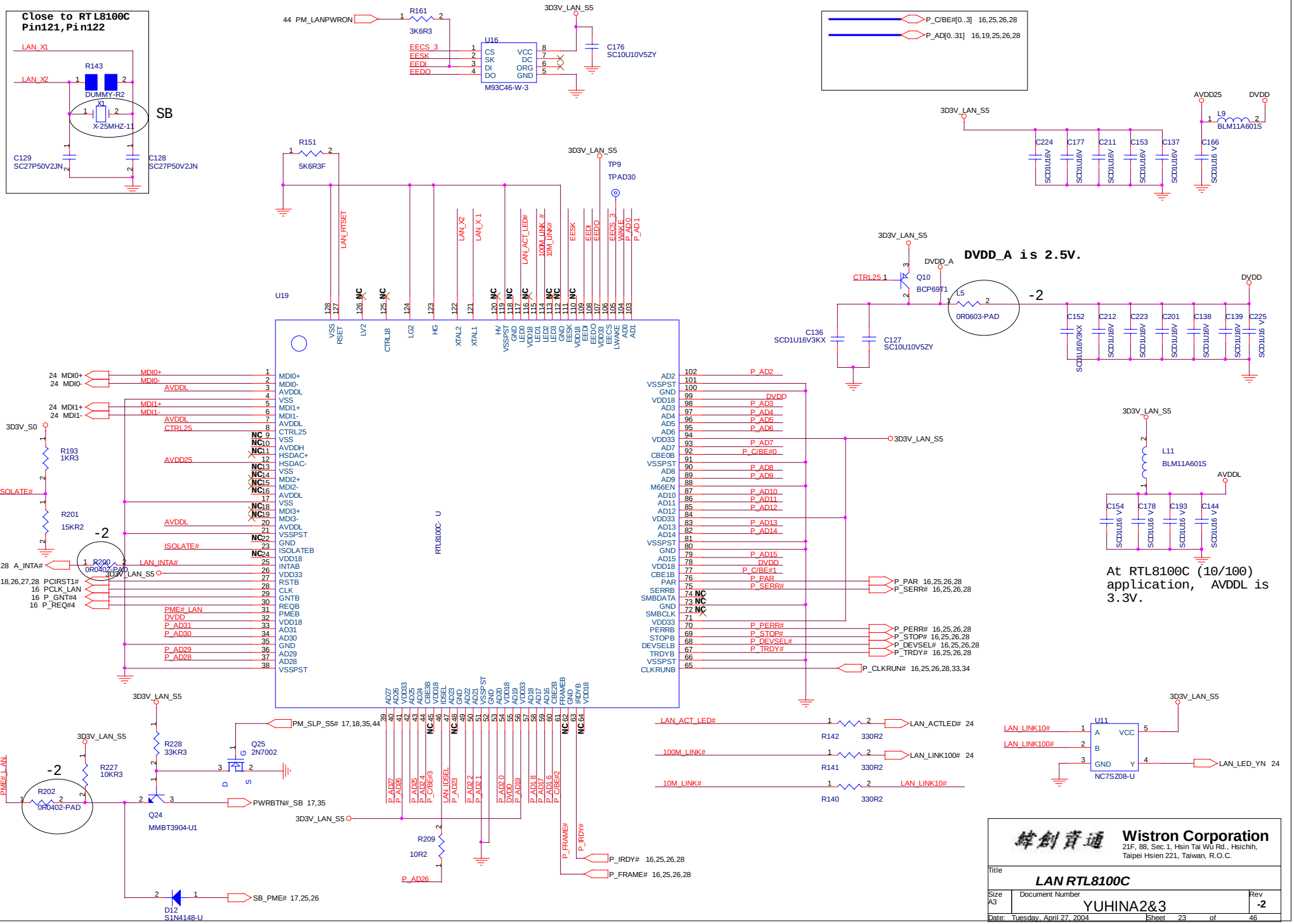




MDC/BT



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***USB and MDC/BT I/F and LAN***	
Size A3	Document Number YUHINA2&3	Rev -2
Date: Thursday, April 08, 2004	Sheet 22 of 46	


Close to RTL8100C Pin121,Pin122
LAN_X1
LAN_X2
R143
DUMMY-R2
X1
X-25MHZ-11
SB
C129 SC27P50V2JN
C128 SC27P50V2JN
44 PM_LANPWRON
R161
3K6R3
U16
EECS_3
EESK
EEDI
EEDO
CS
SK
DI
DO
VCC
DC
ORG
GND
M93C46-W-3
3D3V_LAN_S5
C176 SC10U10V5ZY
P_C/BE#[0..3] 16,25,26,28
P_AD[0..31] 16,19,25,26,28
AVDD25
DVDD
L9 BLM11A601S
C224 C177 C211 C153 C137 C166
SCD1U16V
R151
5K6R3F
TP9
TPAD30
U19
LAN_RTSET
LAN_X2
LAN_X1
LAN_ACT_LED#
100M_LINK_#
10M_LINK#
EESK
EEDI
EEDO
EECS_3
WAKE
P_AD0
P_AD1
VSS RSET LV2 CTRL18 LG2 HG XTAL2 XTAL1 HV VSSPST GND LED0 VDD18 LED1 LED2 GND EESK VDD18 EEDI EEDO VDD33 EECS LWAKE AD0 AD1
DVDD_A is 2.5V.
CTRL25
Q10
BCP69T1
L5
0R0603-PAD
-2
C136 SCD1U16V3KX
C127 SC10U10V5ZY
C152 C212 C223 C201 C138 C139 C225
SCD1U16V3KX
SCD1U16V
MDI0+
MDI0-
MDI1+
MDI1-
AVDDL
CTRL25
AVDD25
ISOLATE#
R193 1KR3
R201 15KR2
R200 0R0402-PAD
LAN_INTA#
PCIRST1#
PCLK_LAN
P_GNT#4
P_REQ#4
PME#_LAN
DVDD
P_AD31
P_AD30
P_AD29
P_AD28
RTL8100C- U
P_AD2
P_AD3
P_AD4
P_AD5
P_AD6
P_AD7
P_C/BE#0
P_AD8
P_AD9
P_AD10
P_AD11
P_AD12
P_AD13
P_AD14
P_AD15
P_C/BE#1
P_PAR
P_SERR#
P_PERR#
P_STOP#
P_DEVSEL#
P_TRDY#
P_CLKRUN# 16,25,26,28,33,34
L11 BLM11A601S
C154 C178 C193 C144
At RTL8100C (10/100) application, AVDDL is 3.3V.
PM_SLP_S5# 17,18,35,44
Q25 2N7002
R228 33KR3
R227 10KR3
R202 0R0402-PAD
Q24 MMBT3904-U1
PWRBTN#_SB 17,35
SB_PME# 17,25,26
D12 S1N4148-U
R209 10R2
P_IRDY# 16,25,26,28
P_FRAME# 16,25,26,28
LAN_ACT_LED#
100M_LINK#
10M_LINK#
R142 330R2
R141 330R2
R140 330R2
LAN_ACTLED# 24
LAN_LINK100# 24
LAN_LINK10#
U11 NC7SZ08-U
LAN_LED_YN 24
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
LAN RTL8100C
Size A3
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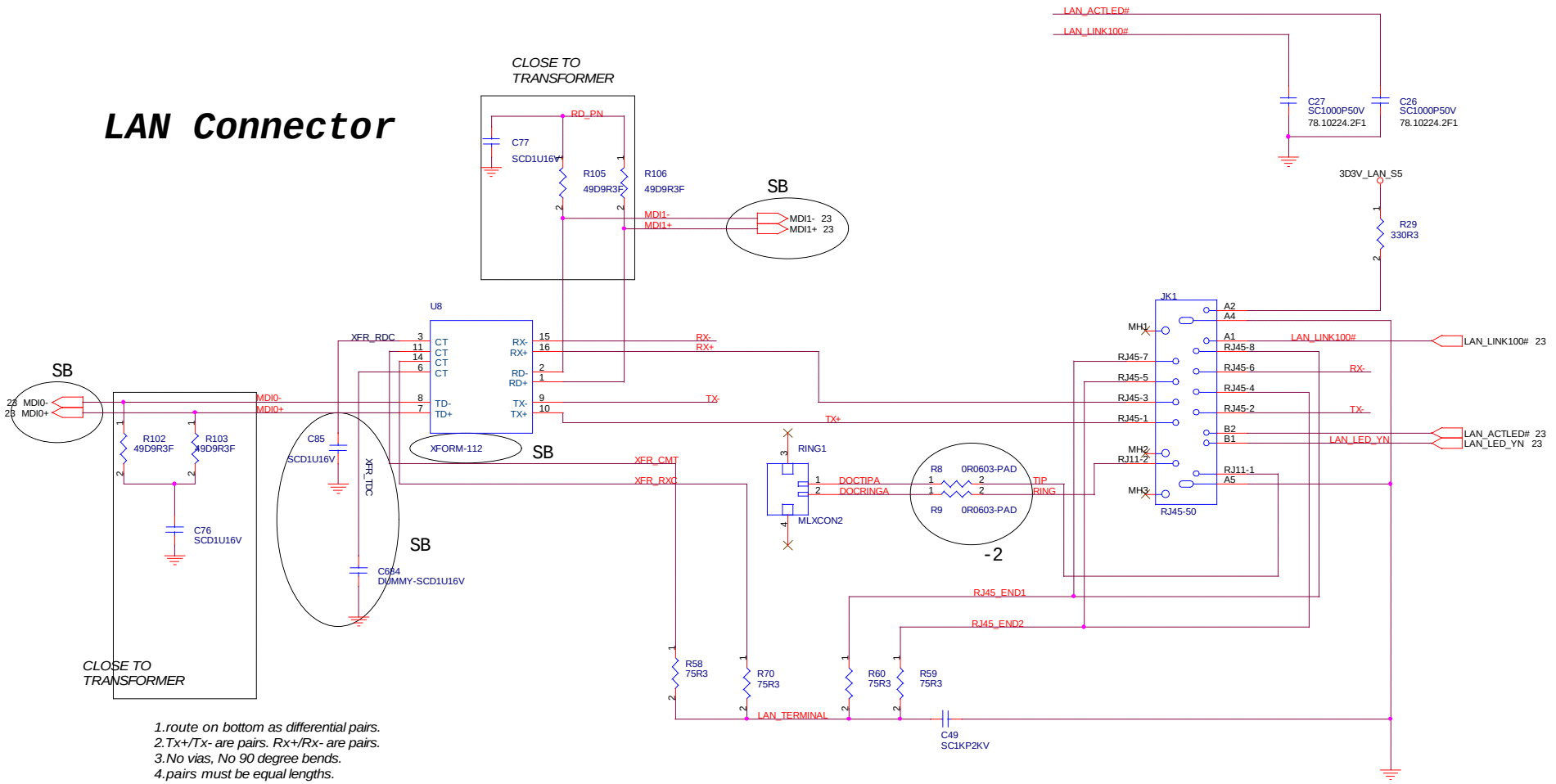
LAN Connector



1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

Green LED---Speed100:O N/Speed10:OFF
Yellow LED---Link:ON ,TX/RX:Flash

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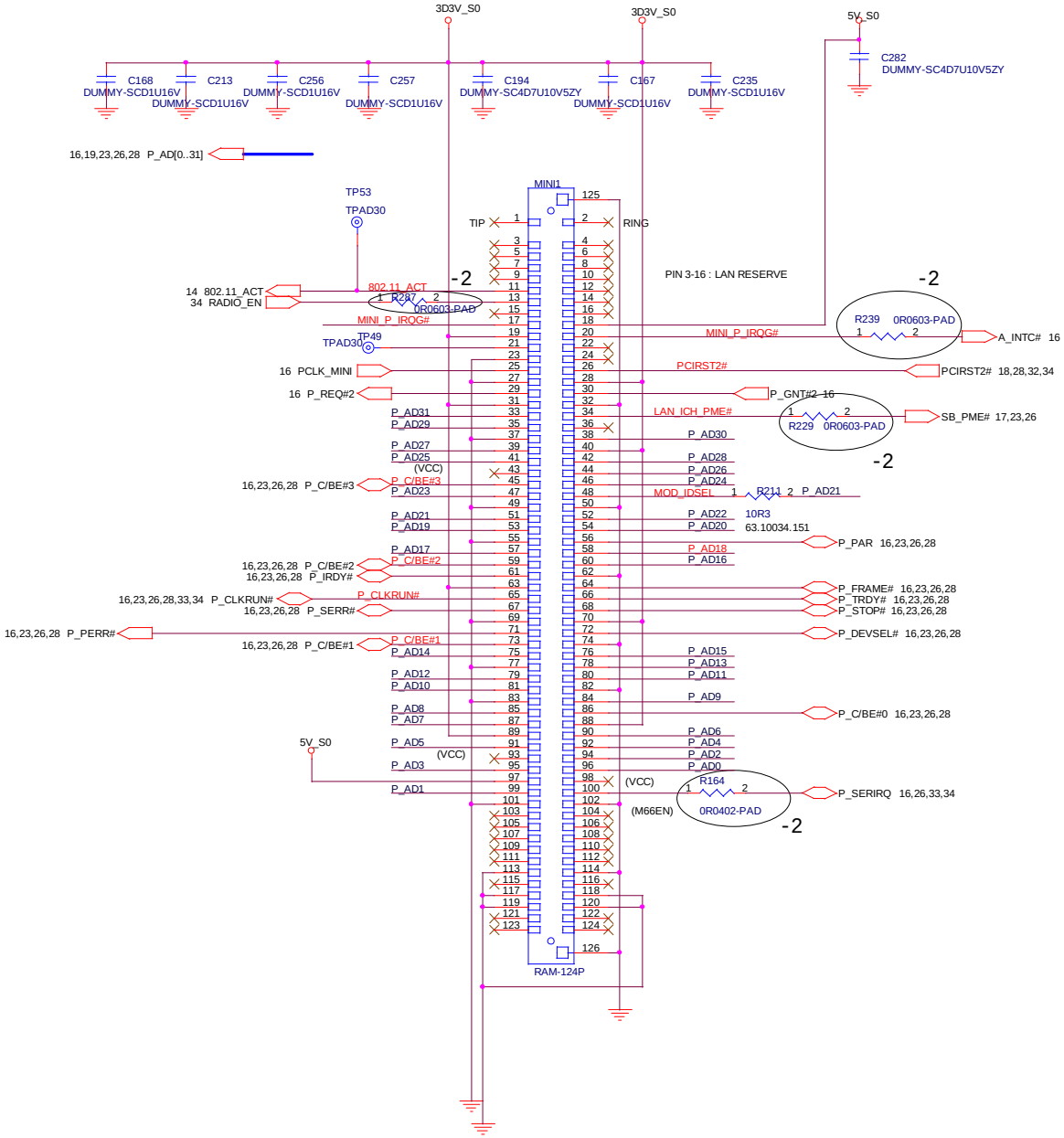
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN Connector
Size: A3 | Document Number: YUHINA2&3 | Rev: -2
Date: Thursday, April 08, 2004 | Sheet 24 of 46

Mini PCI



Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **MINI-PCI**

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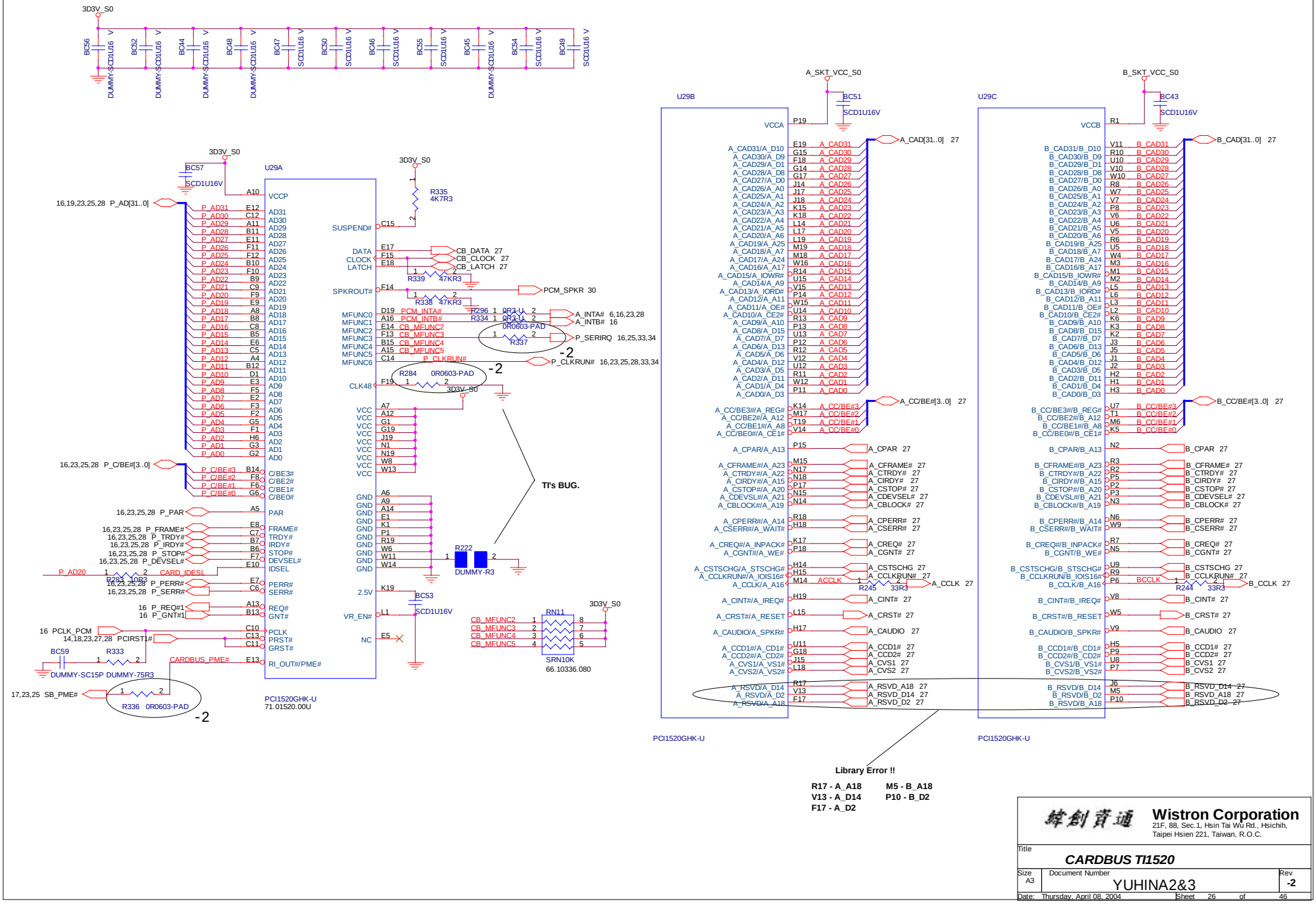
3D3V_S0
BC56 SCD1U16V
BC52 SCD1U16V
BC44 SCD1U16V
BC48 SCD1U16V
BC47 SCD1U16V
BC50 SCD1U16V
BC46 SCD1U16V
BC55 SCD1U16V
BC45 SCD1U16V
BC54 SCD1U16V
BC49 SCD1U16V
DUMMY-SCD1U16V
U29A
PCI1520GHK-U
71.01520.00U
BC57 SCD1U16V
R335 4K7R3
SUSPEND#
DATA
CLOCK
LATCH
CB_DATA 27
CB_CLOCK 27
CB_LATCH 27
R339 47KR3
SPKROUT#
PCM_SPKR 30
R338 47KR3
MFUNC0 PCM_INTA#
MFUNC1 PCM_INTB#
MFUNC2 CB_MFUNC2
MFUNC3 CB_MFUNC3
MFUNC4 CB_MFUNC4
MFUNC5 CB_MFUNC5
MFUNC6 P_CLKRUN#
R296 0R3-U
R334 0R3-U
A_INTA# 6,16,23,28
A_INTB# 16
R337 0R0603-PAD
P_SERIRQ 16,25,33,34
P_CLKRUN# 16,23,25,28,33,34
-2
R284 0R0603-PAD
CLK48
TI's BUG.
R222
DUMMY-R3
BC53 SCD1U16V
2.5V
VR_EN#
NC
RN11
SRN10K
66.10336.080
CB_MFUNC2
CB_MFUNC3
CB_MFUNC4
CB_MFUNC5
R336 0R0603-PAD
17,23,25 SB_PME#
BC59
R333
DUMMY-SC15P
DUMMY-75R3
CARDBUS_PME#
R283 10R3
P_AD20
CARD_IDESL
U29B
U29C
A_SKT_VCC_S0
B_SKT_VCC_S0
BC51 SCD1U16V
BC43 SCD1U16V
A_CAD[31..0] 27
B_CAD[31..0] 27
A_CC/BE#[3..0] 27
B_CC/BE#[3..0] 27
A_CPAR 27
B_CPAR 27
A_CCLK 27
B_CCLK 27
R245 33R3
R244 33R3
ACCLK
BCCLK
Library Error !!
R17 - A_A18
V13 - A_D14
F17 - A_D2
M5 - B_A18
P10 - B_D2
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CARDBUS TI1520
Size A3
Document Number YUHINA2&3
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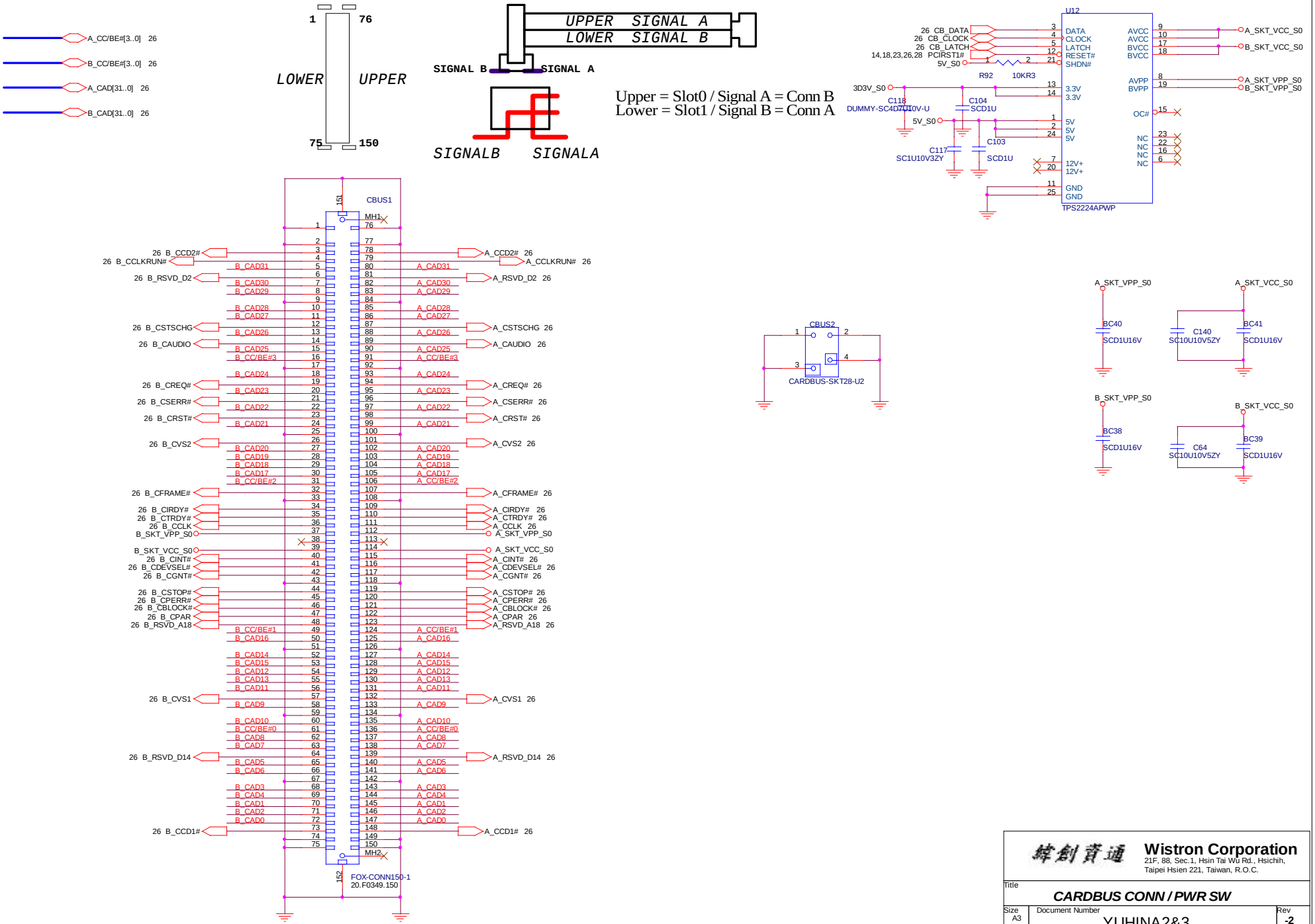
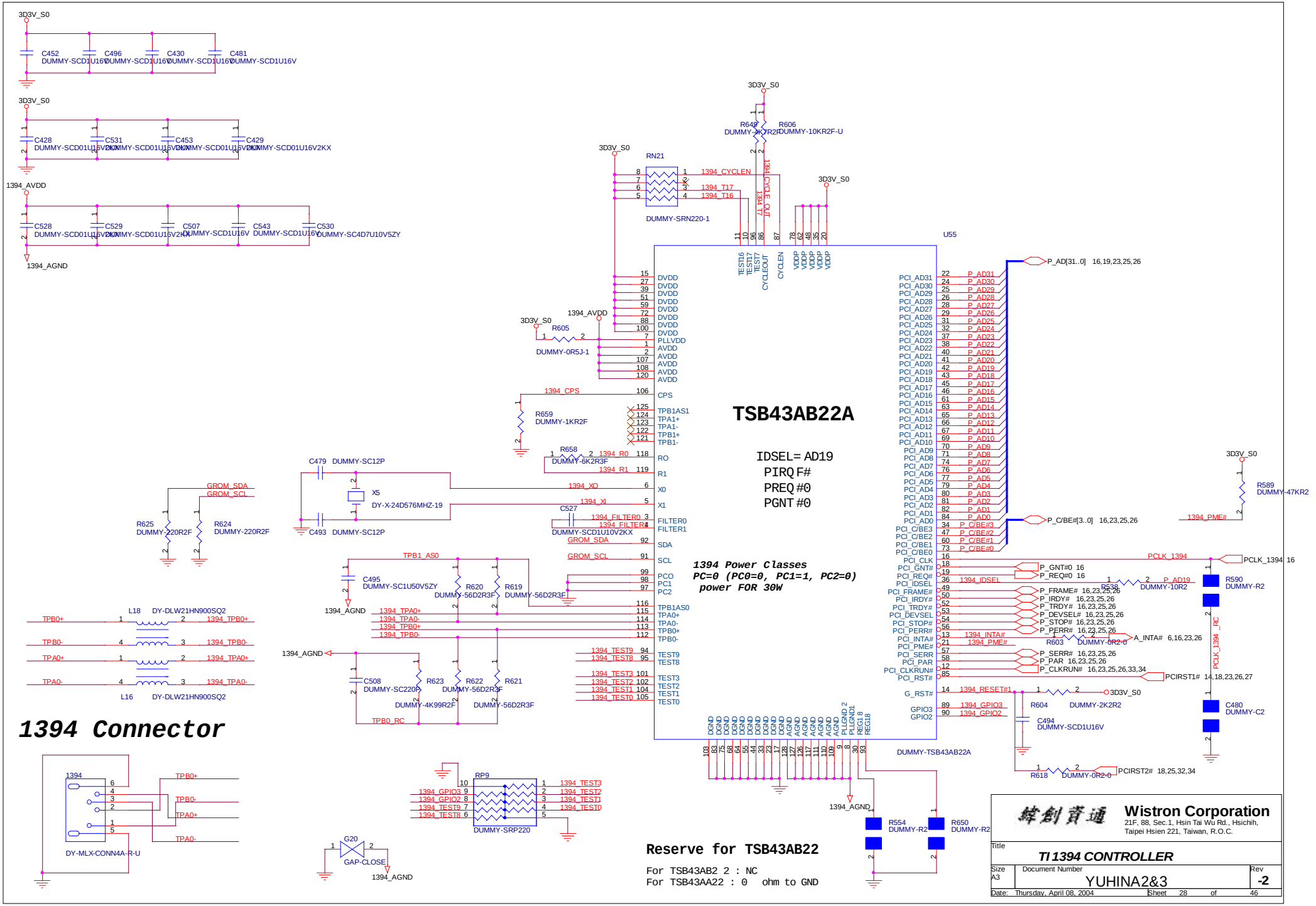


Wistron Corporation		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: CARDBUS CONN / PWR SW		
Size: A3	Document Number: YUHINA2&3	Rev: -2
Date: Thursday, April 08, 2004	Sheet 27 of 46	


TSB43AB22A
IDSEL= AD19
PIRQ F#
PREQ #0
PGNT #0
1394 Power Classes
PC=0 (PC0=0, PC1=1, PC2=0)
power FOR 30W
1394 Connector
Reserve for TSB43AB22
For TSB43AB2 2 : NC
For TSB43AA22 : 0 ohm to GND
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
TI 1394 CONTROLLER
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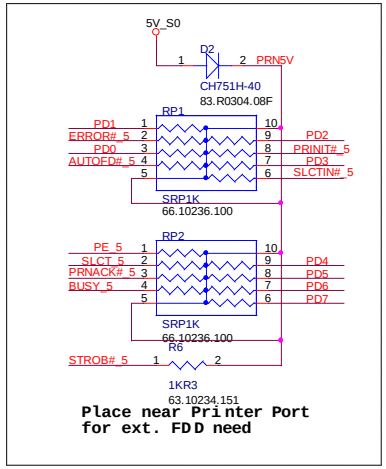
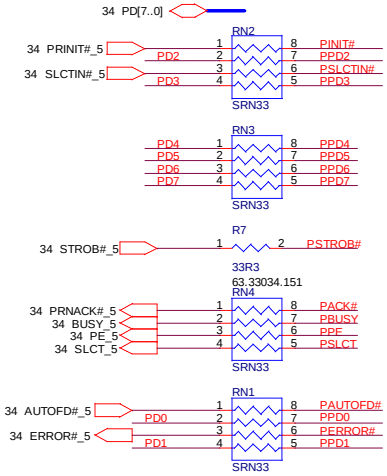
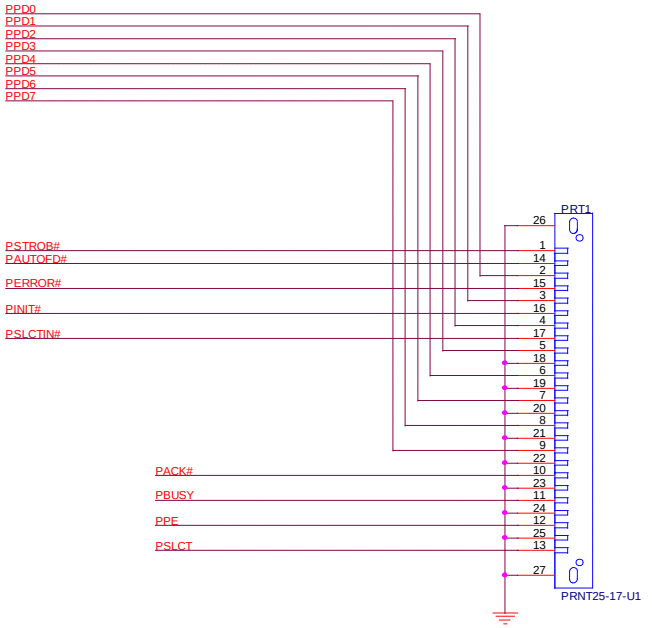
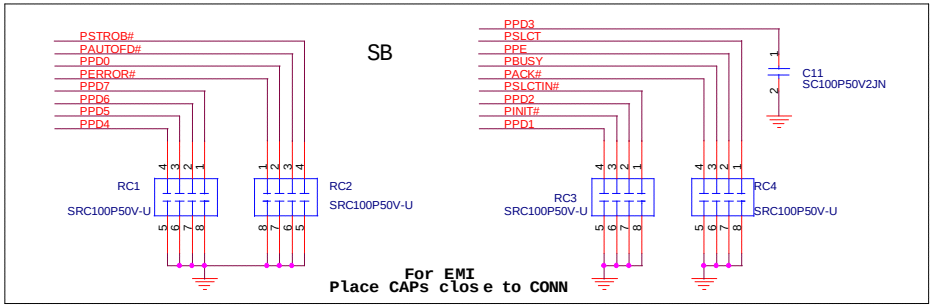
PRINTER PORT









緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Parallel Port***

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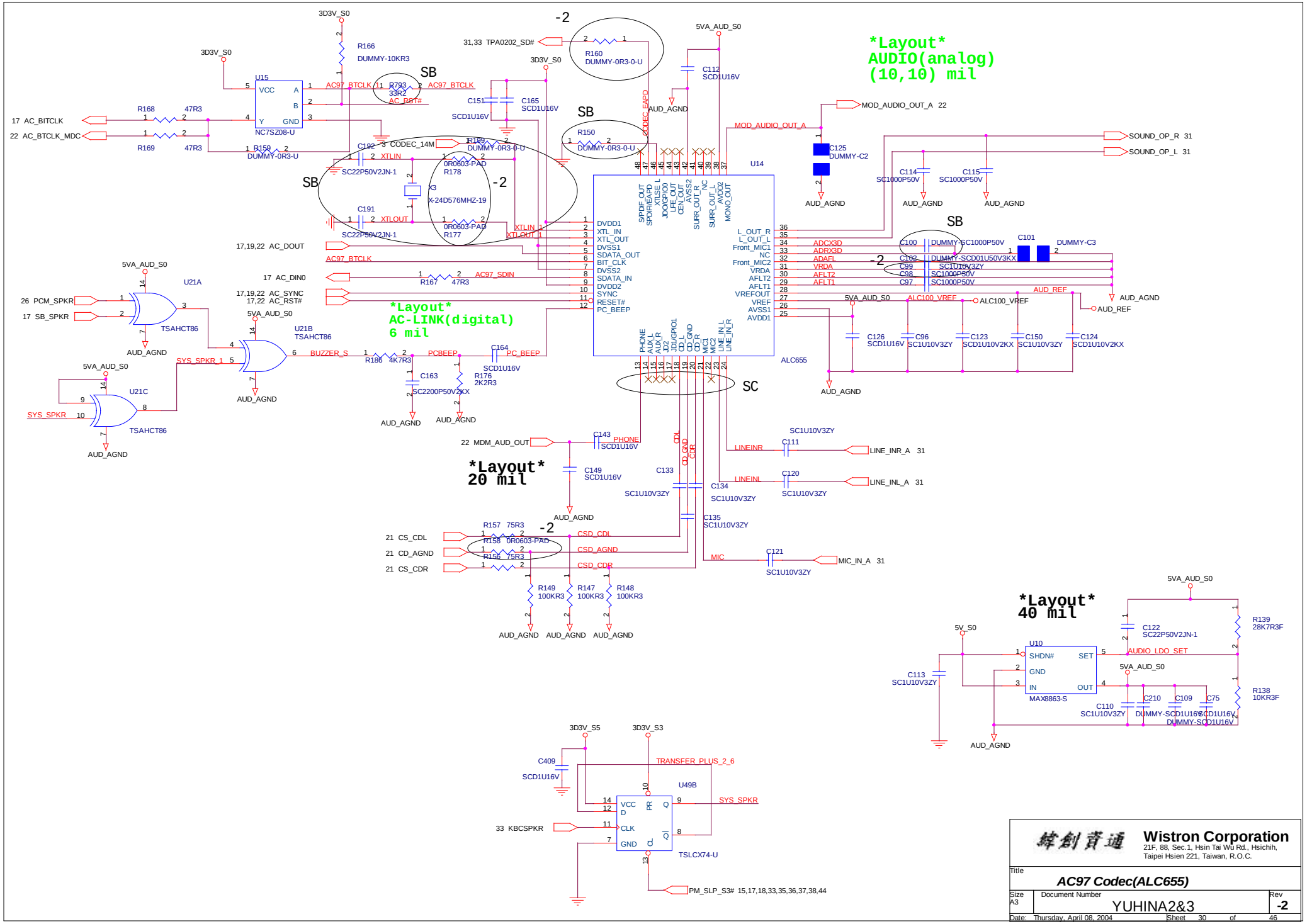
Layout
AUDIO(analog)
(10,10) mil
Layout
AC-LINK(digital)
6 mil
Layout
20 mil
Layout
40 mil
ALC655
U14
U15
NC7SZ08-U
U21A
U21B
U21C
TSAHCT86
U49B
TSLCX74-U
U10
MAX8863-S
SB
SC
-2
3D3V_S0
5VA_AUD_S0
AUD_AGND
5V_S0
3D3V_S5
3D3V_S3
17 AC_BITCLK
22 AC_BTCLK_MDC
17,19,22 AC_DOUT
17 AC_DIN0
17,19,22 AC_SYNC
17,22 AC_RST#
AC97_BTCLK
AC97_SDIN
26 PCM_SPKR
17 SB_SPKR
SYS_SPKR
SYS_SPKR_1
BUZZER_S
PCBEEP
PC_BEEP
22 MDM_AUD_OUT
31,33 TPA0202_SD#
MOD_AUDIO_OUT_A
MOD_AUDIO_OUT_A 22
SOUND_OP_R 31
SOUND_OP_L 31
LINE_INR_A 31
LINE_INL_A 31
MIC_IN_A 31
21 CS_CDL
21 CD_AGND
21 CS_CDR
CSD_CDL
CSD_AGND
CSD_CDR
33 KBCSPKR
PM_SLP_S3# 15,17,18,33,35,36,37,38,44
ALC100_VREF
AUD_REF
AUDIO_LDO_SET
TRANSFER_PLUS_2_6
R166 DUMMY-10KR3
R160 DUMMY-0R3-0-U
R150 DUMMY-0R3-0-U
R159 DUMMY-0R3-0-U
R149 DUMMY-0R3-0-U
R168 47R3
R169 47R3
R167 47R3
R186 4K7R3
R176 2K2R3
R793 33R2
AC_RST#
R178 0R0603-PAD
R177 0R0603-PAD
R158 0R0603-PAD
X-24D576MHZ-19
SC22P50V2JN-1
C112 SCD1U16V
C151 SCD1U16V
C165 SCD1U16V
C164 SCD1U16V
C143 SCD1U16V
C149 SCD1U16V
C409 SCD1U16V
C163 SC2200P50V2KX
C133 SC1U10V3ZY
C134 SC1U10V3ZY
C135 SC1U10V3ZY
C111 SC1U10V3ZY
C120 SC1U10V3ZY
C121 SC1U10V3ZY
C100 DUMMY-SC1000P50V
C101 DUMMY-C3
C102 DUMMY-SCD01U50V3KX
C99 SC1U10V3ZY
C98 SC1000P50V
C97 SC1000P50V
C114 SC1000P50V
C115 SC1000P50V
C125 DUMMY-C2
C126 SCD1U16V
C96 SC1U10V3ZY
C123 SC1U10V2KX
C150 SC1U10V3ZY
C124 SC1U10V2KX
C122 SC22P50V2JN-1
C113 SC1U10V3ZY
C110 SC1U10V3ZY
C210 DUMMY-SCD1U16V
C109 DUMMY-SCD1U16V
C75 SCD1U16V
R139 28K7R3F
R138 10KR3F
R157 75R3
R156 75R3
R149 100KR3
R147 100KR3
R148 100KR3
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
AC97 Codec(ALC655)
Size A3
Document Number
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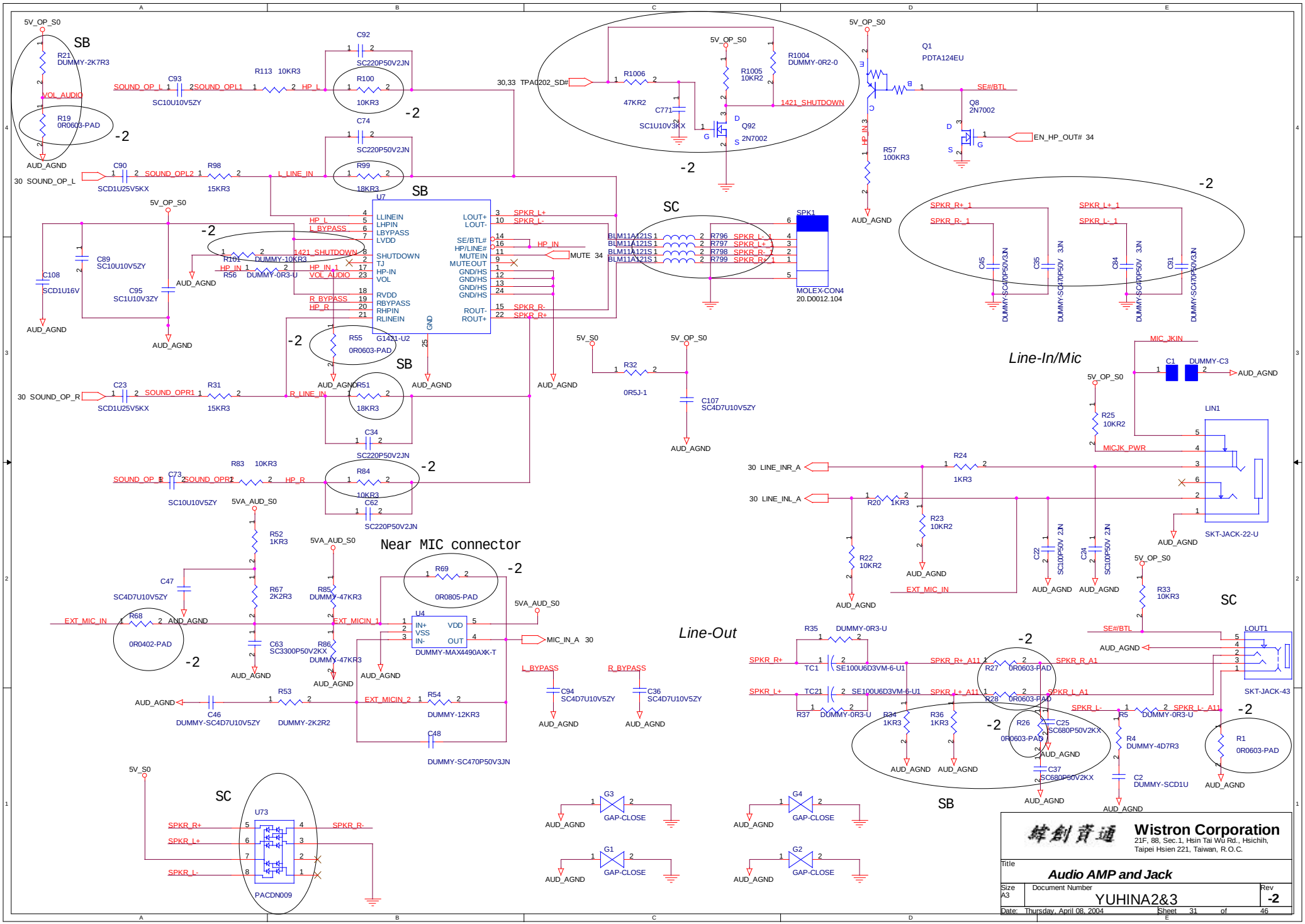
Line-In/Mic
Line-Out
Near MIC connector
SB
SC
-2
U7
LLINEIN
LHPIN
LBYPASS
LVDD
SHUTDOWN
TJ
HP-IN
VOL
RVDD
RBYPASS
RHPIN
RLINEIN
LOUT+
LOUT-
SE/BTL#
HP/LINE#
MUTEIN
MUTEOUT
GND/HS
ROUT-
ROUT+
U4
IN+
IN-
VSS
VDD
OUT
DUMMY-MAX4490AXK-T
U73
PACDN009
Q1
PDTA124EU
Q8
2N7002
Q92
2N7002
SPK1
MOLEX-CON4
20.D0012.104
MIC_JKIN
LIN1
SKT-JACK-22-U
LOUT1
SKT-JACK-43
G1
G2
G3
G4
GAP-CLOSE
5V_OP_S0
5V_S0
5VA_AUD_S0
AUD_AGND
SOUND_OP_L
SOUND_OP_R
L_LINE_IN
R_LINE_IN
HP_L
HP_R
MUTE 34
EN_HP_OUT# 34
SE#/BTL
EXT_MIC_IN
MIC_IN_A 30
30 LINE_INR_A
30 LINE_INL_A
SPKR_L+
SPKR_L-
SPKR_R+
SPKR_R-
L_BYPASS
R_BYPASS
1421_SHUTDOWN
TPA0202_SD#
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Audio AMP and Jack
YUHINA2&3
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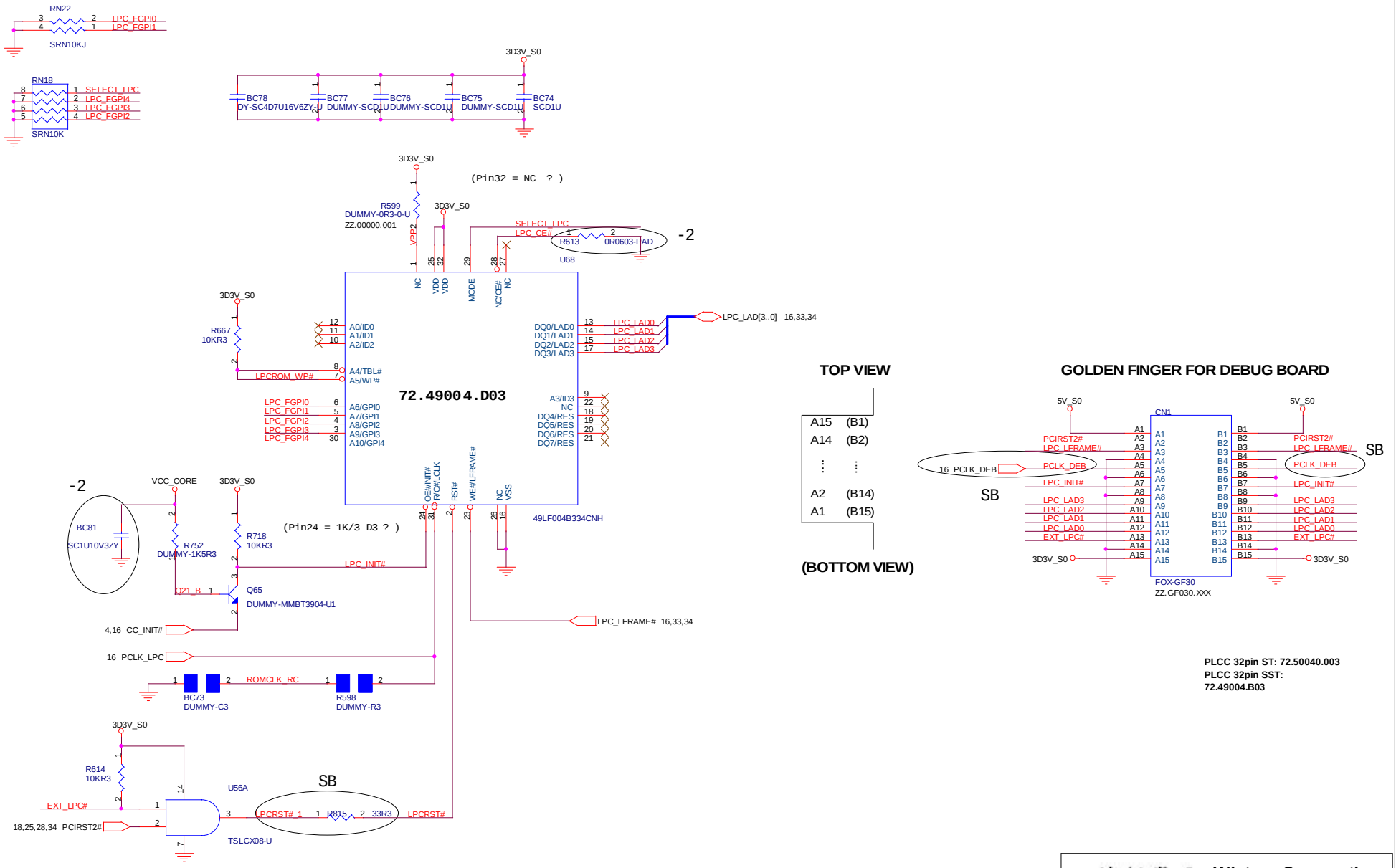
RN22
LPC_FGPI0
LPC_FGPI1
SRN10KJ
RN18
SELECT_LPC
LPC_FGPI4
LPC_FGPI3
LPC_FGPI2
SRN10K
3D3V_S0
BC78
DY-SC4D7U16V6ZY-U
BC77
DUMMY-SCD1U
BC76
DUMMY-SCD1U
BC75
DUMMY-SCD1U
BC74
SCD1U
(Pin32 = NC ?)
R599
DUMMY-0R3-0-U
ZZ.00000.001
VPP2
SELECT_LPC
LPC_CE#
R613
0R0603-PAD
-2
U68
NC
VDD
VDD
MODE
NC/CE#
NC
R667
10KR3
LPCROM_WP#
A0/ID0
A1/ID1
A2/ID2
A4/TBL#
A5/WP#
72.49004.D03
A6/GPI0
A7/GPI1
A8/GPI2
A9/GPI3
A10/GPI4
DQ0/LAD0
DQ1/LAD1
DQ2/LAD2
DQ3/LAD3
LPC_LAD[3..0] 16,33,34
A3/ID3
NC
DQ4/RES
DQ5/RES
DQ6/RES
DQ7/RES
OE#/INIT#
R/C#/LCLK
RST#
WE#/LFRAME#
NC
VSS
49LF004B334CNH
LPC_LFRAME# 16,33,34
-2
VCC_CORE
BC81
SC1U10V3ZY
R752
DUMMY-1K5R3
R718
10KR3
(Pin24 = 1K/3 D3 ?)
LPC_INIT#
Q21_B
Q65
DUMMY-MMBT3904-U1
4,16 CC_INIT#
16 PCLK_LPC
ROMCLK_RC
BC73
DUMMY-C3
R598
DUMMY-R3
R614
10KR3
U56A
SB
EXT_LPC#
18,25,28,34 PCIRST2#
LPCRST#_1
R815
33R3
LPCRST#
TSLCX08-U
TOP VIEW
A15 (B1)
A14 (B2)
A2 (B14)
A1 (B15)
(BOTTOM VIEW)
GOLDEN FINGER FOR DEBUG BOARD
5V_S0
CN1
PCIRST2#
LPC_LFRAME#
PCLK_DEB
LPC_INIT#
LPC_LAD3
LPC_LAD2
LPC_LAD1
LPC_LAD0
EXT_LPC#
3D3V_S0
16 PCLK_DEB
SB
FOX-GF30
ZZ.GF030.XXX
PLCC 32pin ST: 72.50040.003
PLCC 32pin SST:
72.49004.B03
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
LPC and Debug
Size
A3
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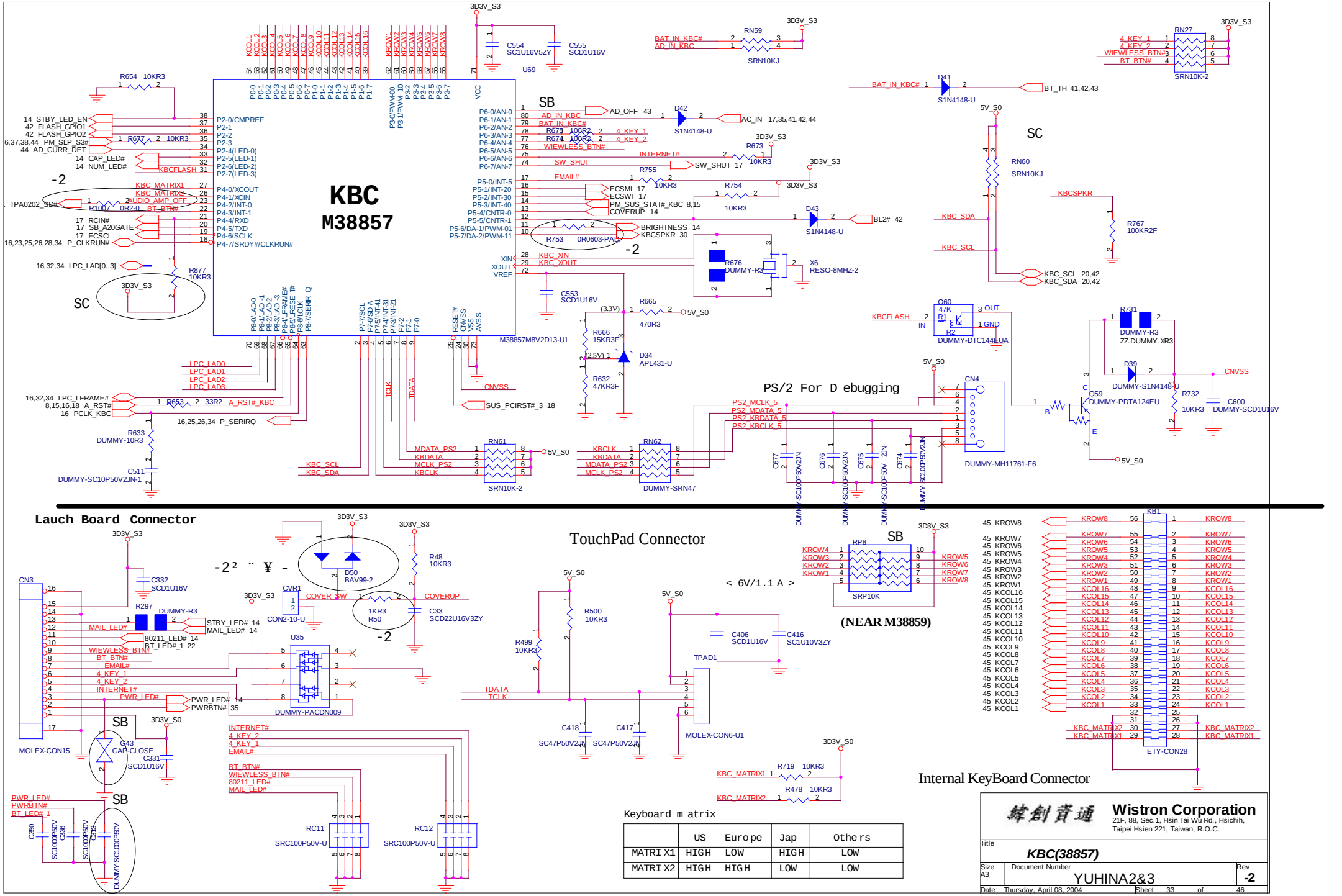
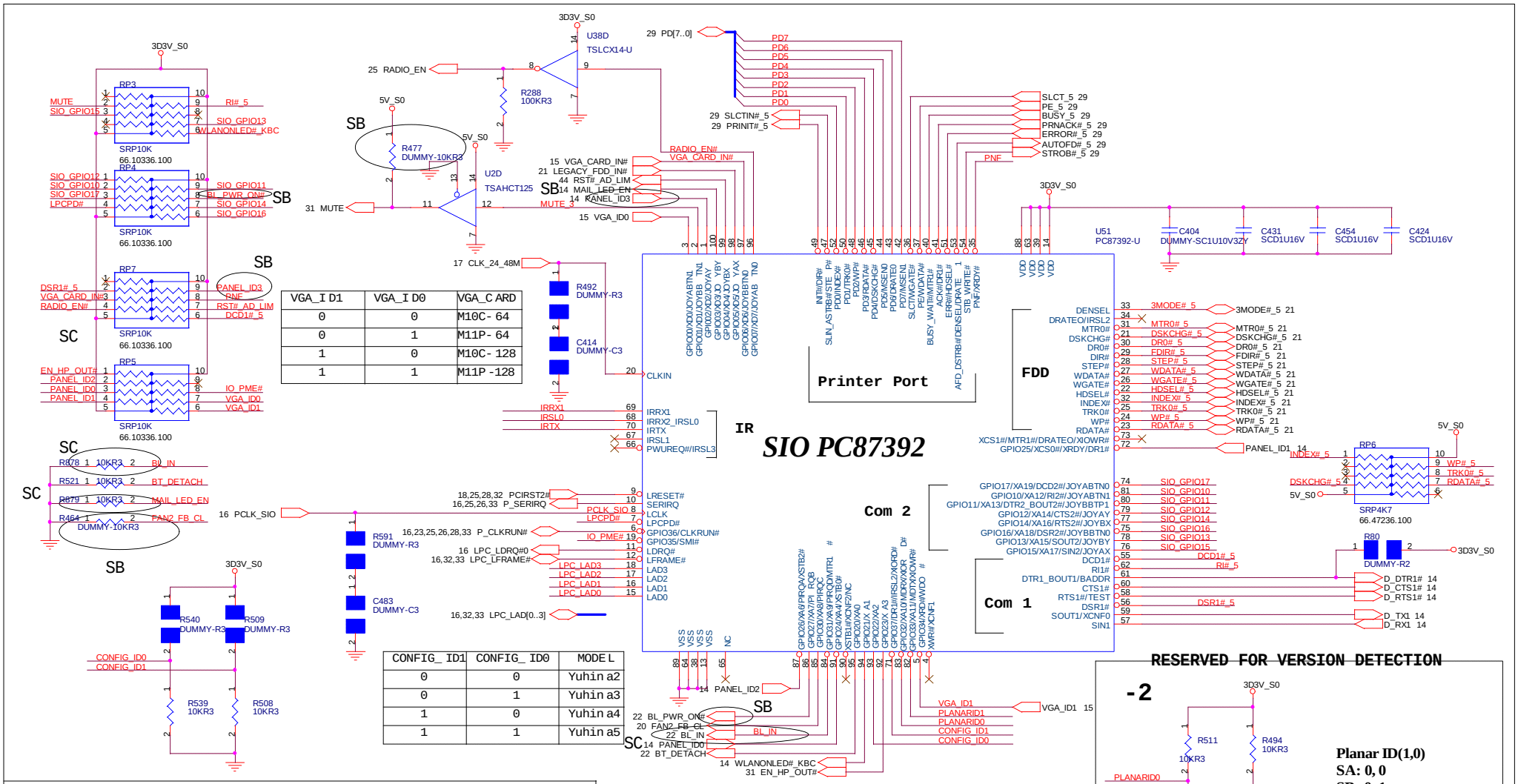


	US	Europe	Jap	Others
MATRIX1	HIGH	LOW	HIGH	LOW
MATRIX2	HIGH	HIGH	LOW	LOW



VGA_ID1	VGA_ID0	VGA_CARD
0	0	M10C-64
0	1	M11P-64
1	0	M10C-128
1	1	M11P-128

CONFIG_ID1	CONFIG_ID0	MODEL
0	0	Yuhina2
0	1	Yuhina3
1	0	Yuhina4
1	1	Yuhina5

Infineon FIR Module

Layout Guide:
(1) FIR_5V : 30 mils

U82
C640 SCD1U16V
C671 SC10U10V5ZY
VCC2/IRED_ANODE
IRED_CATHODE
TXD
RXD
SD
VCC1
MODE
GND
IRTX
IRRX1
IRSL0
FIR-TFDU6102

PANEL_ID3	PANEL_ID2	PANEL_ID1	PANEL_ID0	VENDORS
	PANEL_ID D EFINE			
0	0	0	0	15" SXGA+
0	0	0	1	Hydis (14")SPWG
0	0	1	0	15" WIDE
0	0	1	1	Hitachi (15")
0	0	1	1	AU (15")
0	0	1	1	CMO(15")
0	1	0	0	CMO(14")
0	1	0	1	AU (14")
0	1	1	0	AU (14")**
0	1	1	1	No Panel
	Note : AU (¤ ¹),CMO(© ¬),** : With Digitizer			

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Title: SIO(87392)

Size	Document Number	Rev
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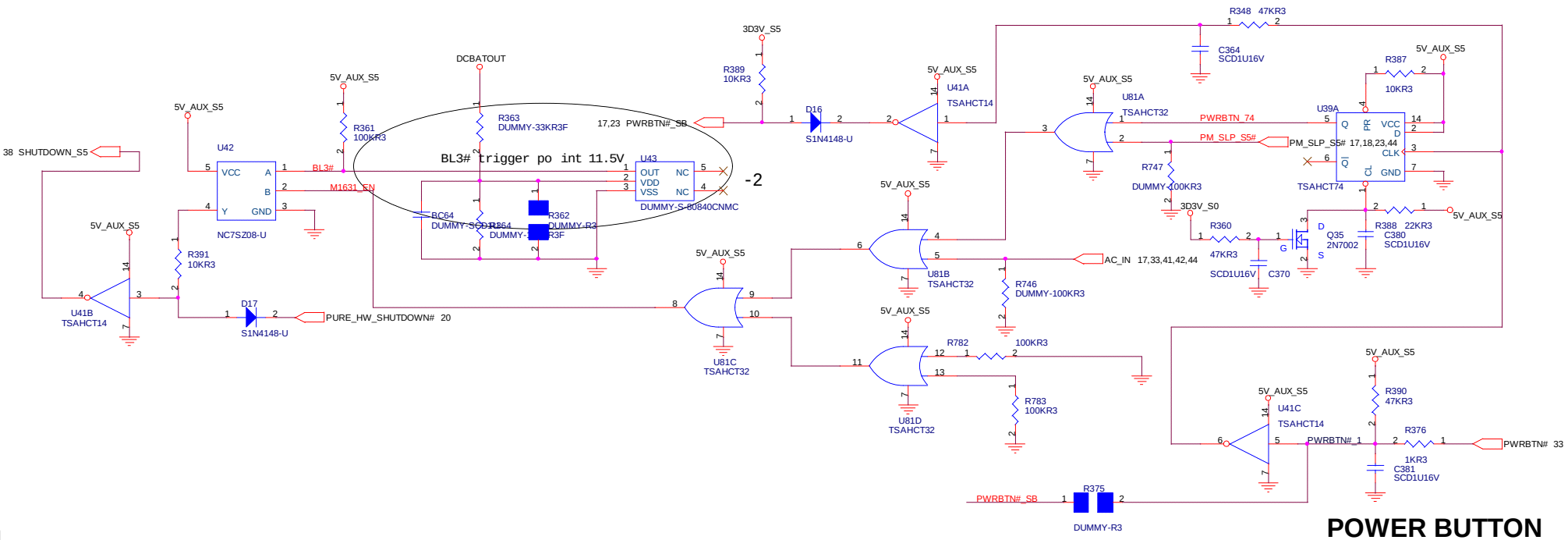
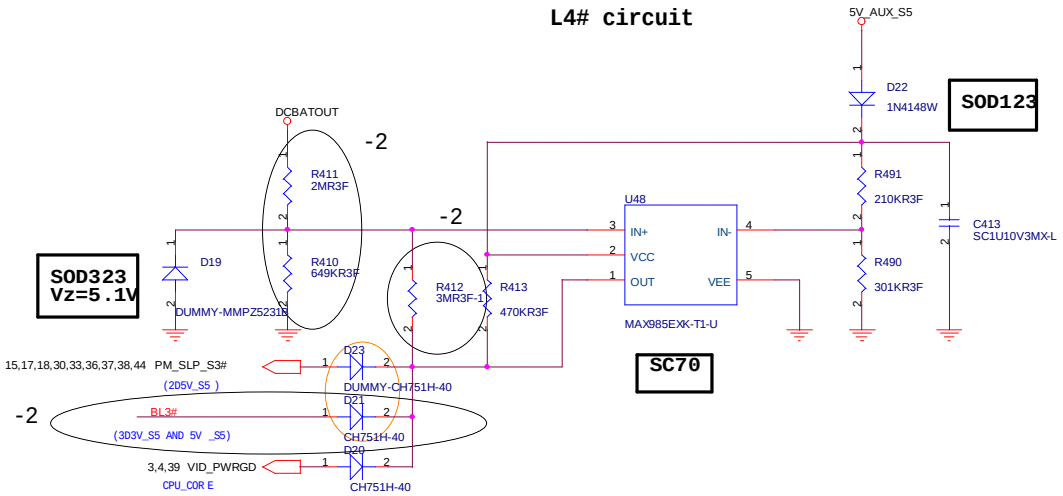
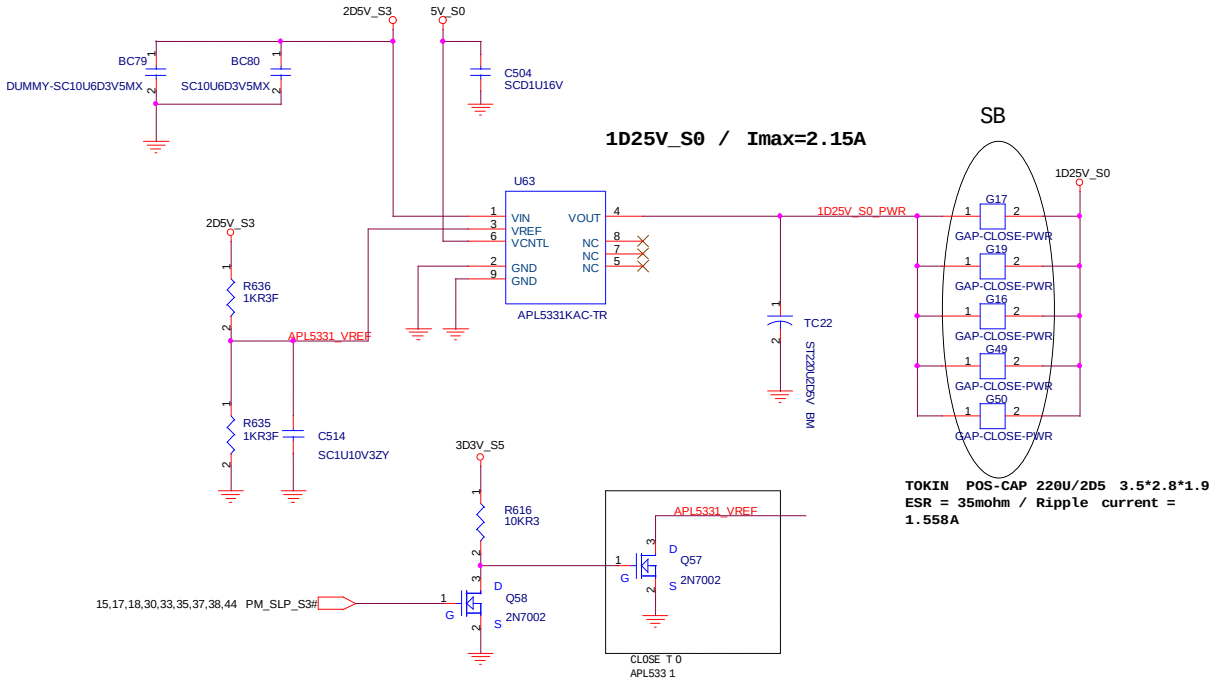
Date: Thursday, April 08, 2004 Sheet 34 of 46

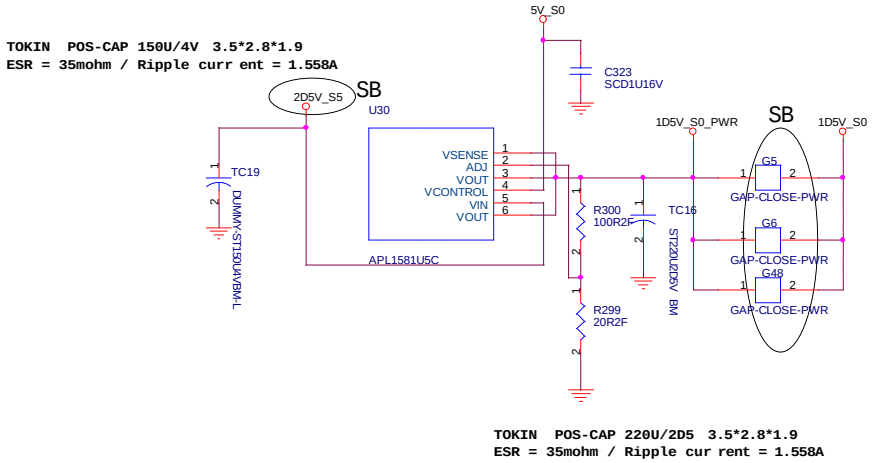


POWER BUTTON



蜂創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***POWER ON CIRCUIT***	
Size A3	Document Number YUHINA2&3	Rev **-2**
Date: Thursday, April 08, 2004	Sheet 35 of 46	





Wistron Corporation		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: 1D25V_S0_APL5331 / 1D5V_S0_APL1581/L4		
Size: A3	Document Number: YUHINA2&3	Rev: -2
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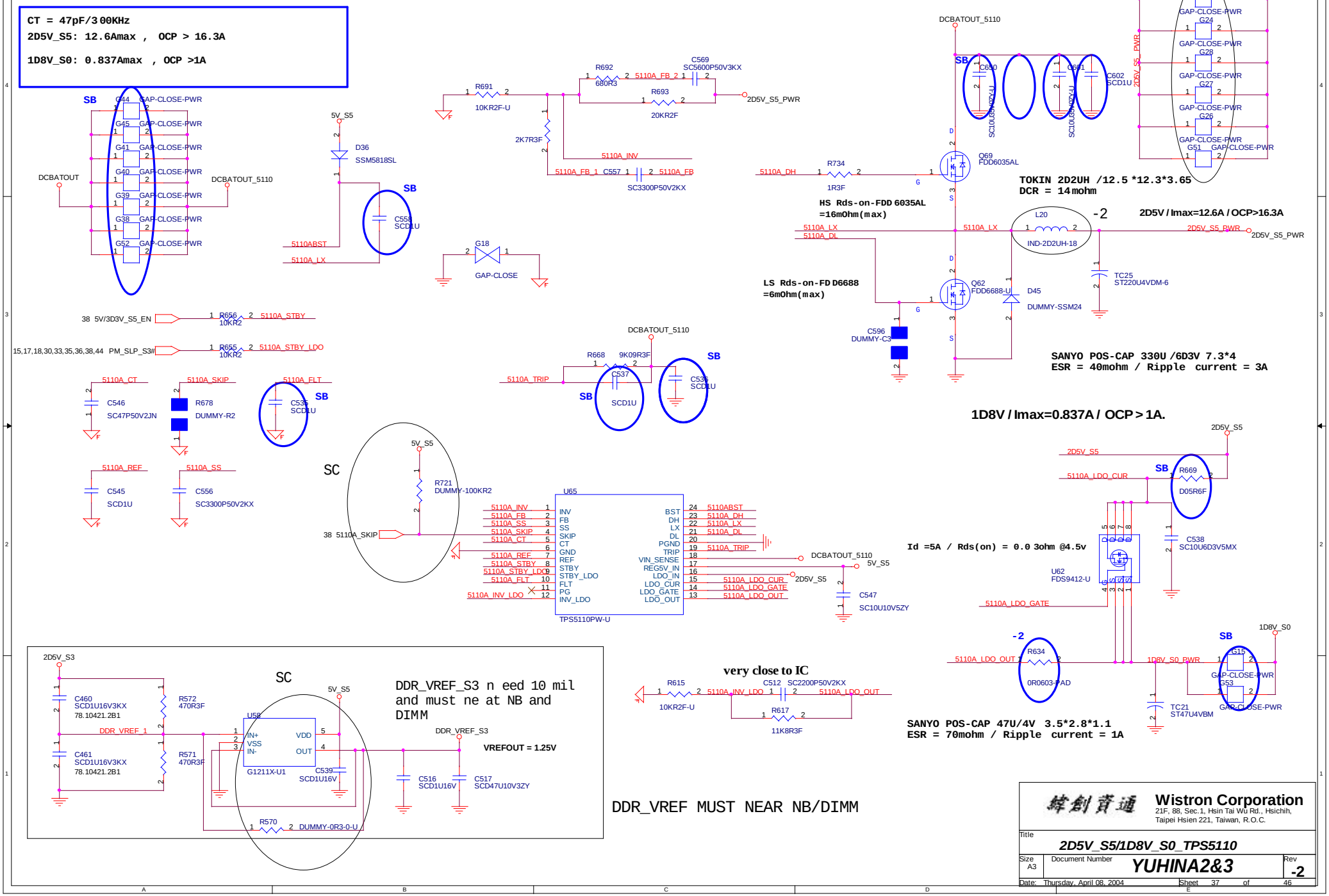
TI TPS5110 for 2.5V and 1.8V

CT = 47pF/300KHz
2D5V_S5: 12.6Amax , OCP > 16.3A
1D8V_S0: 0.837Amax , OCP >1A



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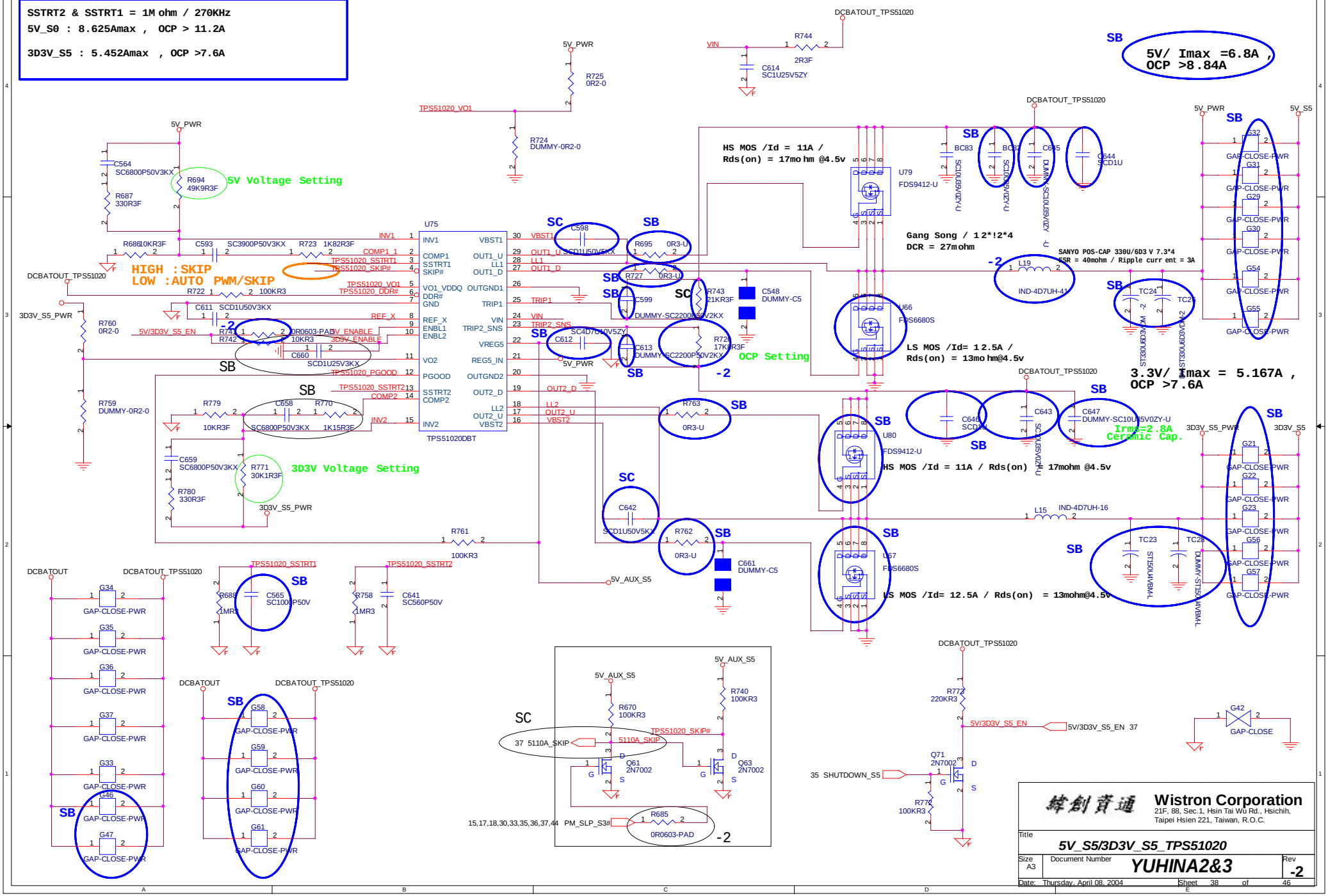
Title	2D5V_S5/1D8V_S0_TPS5110	
Size A3	Document Number YUHINA2&3	Rev -2
Date: Thursday, April 08, 2004	Sheet 37 of 46	

TI TPS51020 for 5V and 3D3V

SSTRT2 & SSTRT1 = 1M ohm / 270KHz
5V_S0 : 8.625Amax , OCP > 11.2A

3D3V_S5 : 5.452Amax , OCP >7.6A



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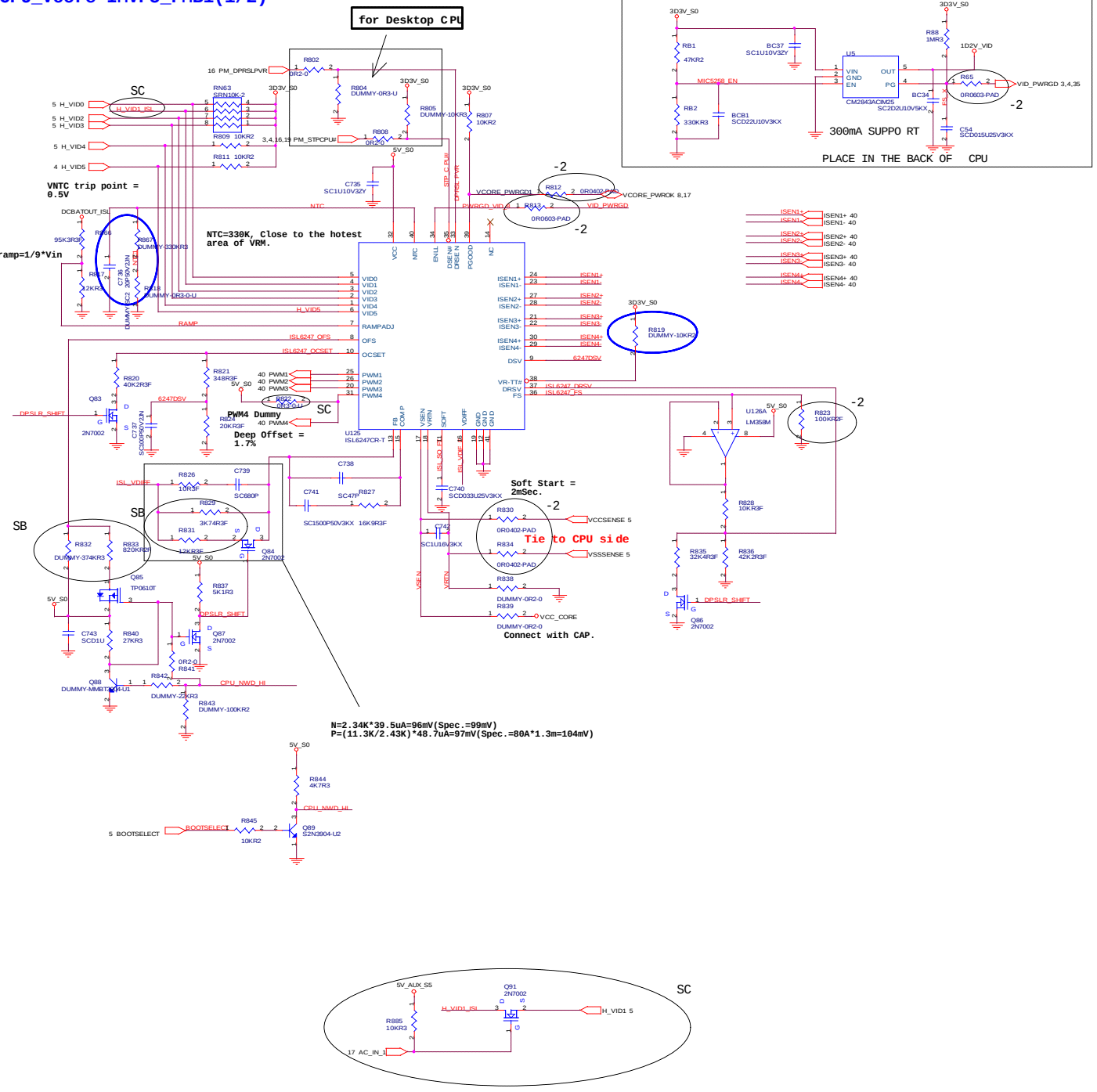
Title	5V_S5/3D3V_S5_TPS51020		
Size A3	Document Number YUHINA2&3	Rev -2	
Date: Thursday, April 08, 2004	Sheet 38 of 46		

CPU_Vcore IMVP5_FMB1(1/2)



Voltage Identication Codes

VID5	VID4	VID3	VID2	VID1	VID0	VDAC
X	1	1	1	1	1	OFF
0	0	1	0	1	0	0.8375
1	0	1	0	0	1	0.8500
0	0	1	0	0	1	0.8625
1	0	1	0	0	0	0.8750
0	0	1	0	0	0	0.8875
1	0	0	1	1	1	0.9000
0	0	0	1	1	1	0.9125
1	0	0	1	1	0	0.9250
0	0	0	1	1	0	0.9375
1	0	0	1	0	1	0.9500
0	0	0	1	0	1	0.9625
1	0	0	1	0	0	0.9750
0	0	0	1	0	0	0.9875
1	0	0	0	1	1	1.0000
0	0	0	0	1	1	1.0125
1	0	0	0	1	0	1.0250
0	0	0	0	1	0	1.0375
1	0	0	0	0	1	1.0500
0	0	0	0	0	1	1.0625
1	0	0	0	0	0	1.0750
0	0	0	0	0	0	1.0875
1	1	1	1	1	0	1.1000
0	1	1	1	1	0	1.1125
1	1	1	1	0	1	1.1250
0	1	1	1	0	1	1.1375
1	1	1	1	0	0	1.1500
0	1	1	1	0	0	1.1625
1	1	1	0	1	1	1.1750
0	1	1	0	1	1	1.1875
1	1	1	0	1	0	1.2000
0	1	1	0	1	0	1.2125
1	1	1	0	0	1	1.2250
0	1	1	0	0	1	1.2375
1	1	1	0	0	0	1.2500
0	1	1	0	0	0	1.2625
1	1	0	1	1	1	1.2750
0	1	0	1	1	1	1.2875
1	1	0	1	1	0	1.3000
0	1	0	1	1	0	1.3125
1	1	0	1	0	1	1.3250
0	1	0	1	0	1	1.3375
1	1	0	1	0	0	1.3500
0	1	0	1	0	0	1.3625
1	1	0	0	1	1	1.3750
0	1	0	0	1	1	1.3875
1	1	0	0	1	0	1.4000
0	1	0	0	1	0	1.4125
1	1	0	0	0	1	1.4250
0	1	0	0	0	1	1.4375
1	1	0	0	0	0	1.4500
0	1	0	0	0	0	1.4625
1	0	1	1	1	1	1.4750

Voltage Identication Codes

VID5	VID4	VID3	VID2	VID1	VID0	VDAC
	0	1	1	1	1	1.4875
	0	1	1	1	0	1.5000
	0	1	1	1	0	1.5125
	0	1	1	0	1	1.5250
	0	1	1	0	1	1.5375
	0	1	1	0	0	1.5500
	0	1	1	0	0	1.5625
	0	1	0	1	1	1.5750
	0	1	0	1	1	1.5875
	0	1	0	1	0	1.6000

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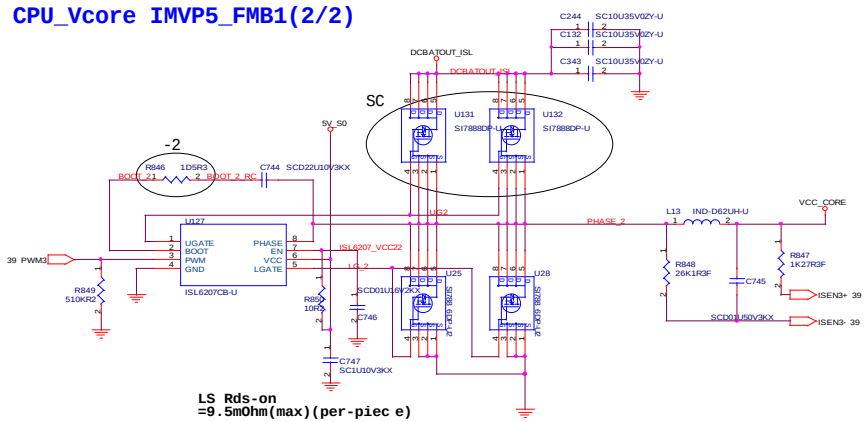
Title: CPU_Vcore IMVP5_FMB1(1/2)

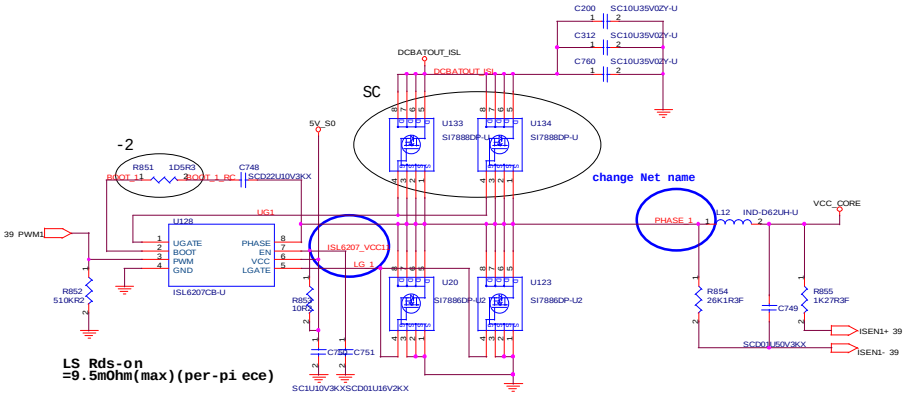
Size: A2 | Document Number: YUHINA2&3 | Rev: -2

Date: Thursday, April 08, 2004 | Sheet 39 of 46

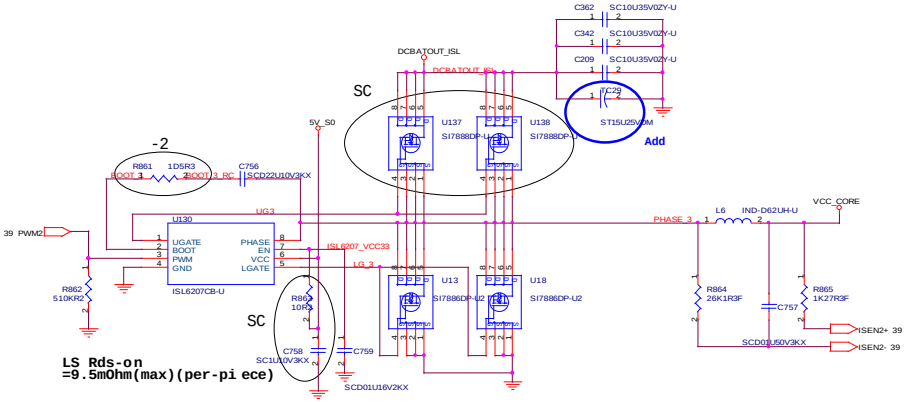
CPU_Vcore IMVP5_FMB1(2/2)



LS Rds-on
=9.5mOhm(max)(per-piec e)

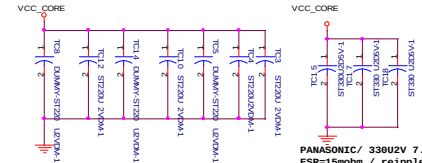


LS Rds-on
=9.5mOhm(max)(per-pi ece)



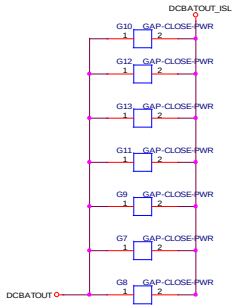
LS Rds-on
=9.5mOhm(max)(per-pi ece)

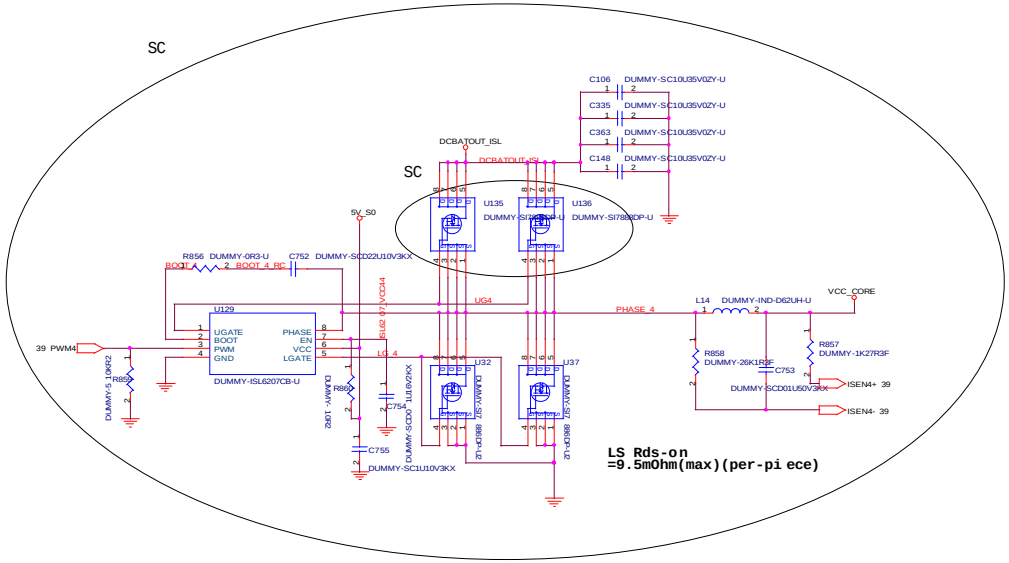
PLACE IN THE BACK OF CPU, ESR < (TBD)mOhm,



PANASONIC/ 330U2V 7. 3*4.3*1.9
ESR=9mohm / reipple current
=3A

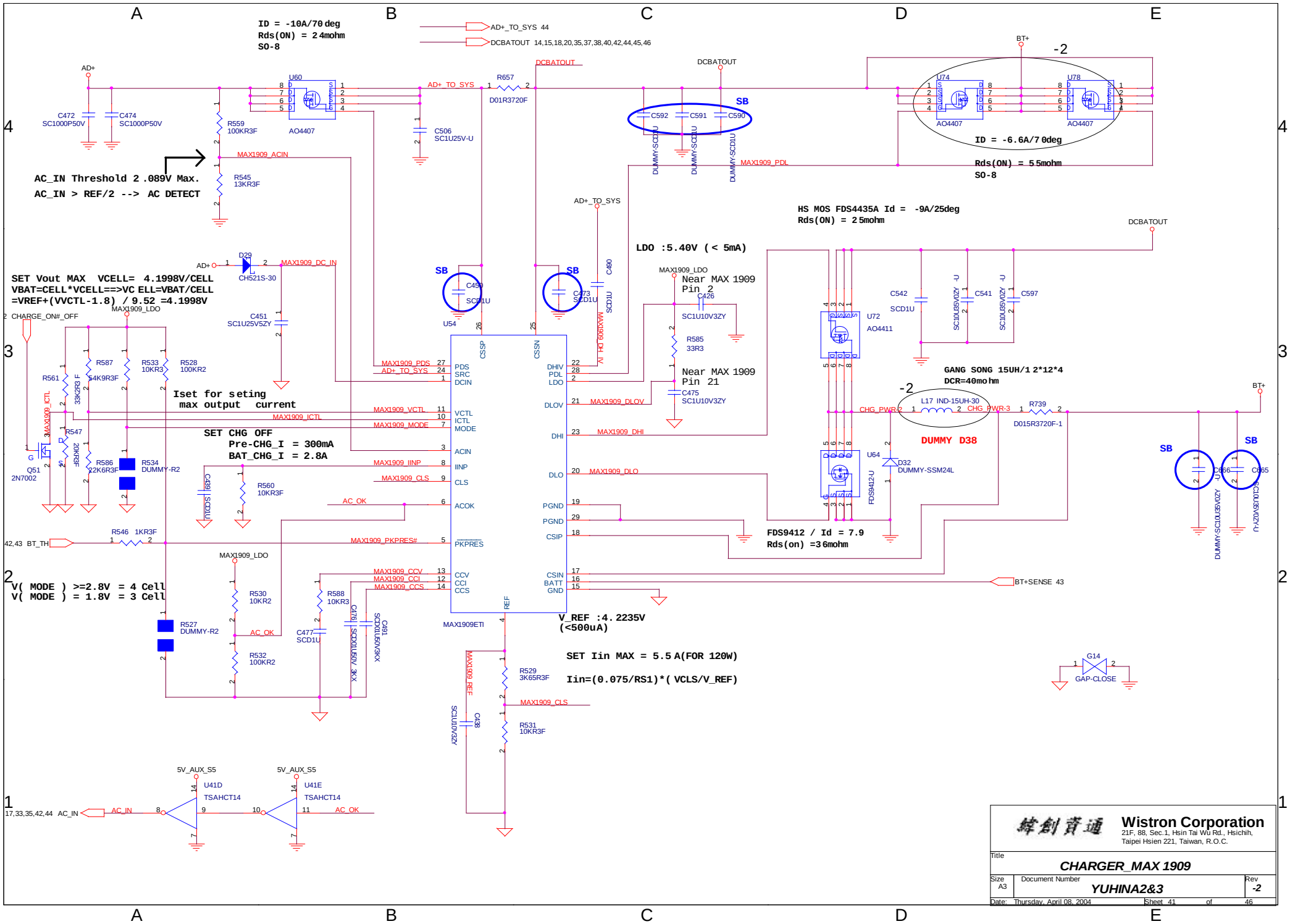
PANASONIC/ 330U2V 7.3 *4.3*1.9
ESR=15mohm / reipple current
=3.1A





LS Rds-on
=9.5mOhm(max)(per-pi ece)

華創資通	Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	CPU_Vcore IMVP5_FMB1(2/2)	
Size A2	Document Number YUHINA2&3	Rev -2
Date: Thursday, April 08, 2004	Sheet 40 of 46	


ID = -10A/70 deg
Rds(ON) = 24mohm
SO-8
AD+_TO_SYS 44
DCBATOUT 14,15,18,20,35,37,38,40,42,44,45,46
AC_IN Threshold 2.089V Max.
AC_IN > REF/2 --> AC DETECT
SET Vout MAX VCELL= 4.1998V/CELL
VBAT=CELL*VCELL==>VC ELL=VBAT/CELL
=VREF+(VVCTL-1.8) / 9.52 =4.1998V
Iset for seting
max output current
SET CHG OFF
Pre-CHG_I = 300mA
BAT_CHG_I = 2.8A
V(MODE) >=2.8V = 4 Cell
V(MODE) = 1.8V = 3 Cell
LDO :5.40V (< 5mA)
HS MOS FDS4435A Id = -9A/25deg
Rds(ON) = 25mohm
ID = -6.6A/70deg
Rds(ON) = 55mohm
SO-8
GANG SONG 15UH/12*12*4
DCR=40mohm
DUMMY D38
FDS9412 / Id = 7.9
Rds(on) =36mohm
V_REF :4.2235V
(<500uA)
SET Iin MAX = 5.5A(FOR 120W)
Iin=(0.075/RS1)*(VCLS/V_REF)
Near MAX 1909 Pin 2
Near MAX 1909 Pin 21
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.
CHARGER_MAX 1909
YUHINA2&3
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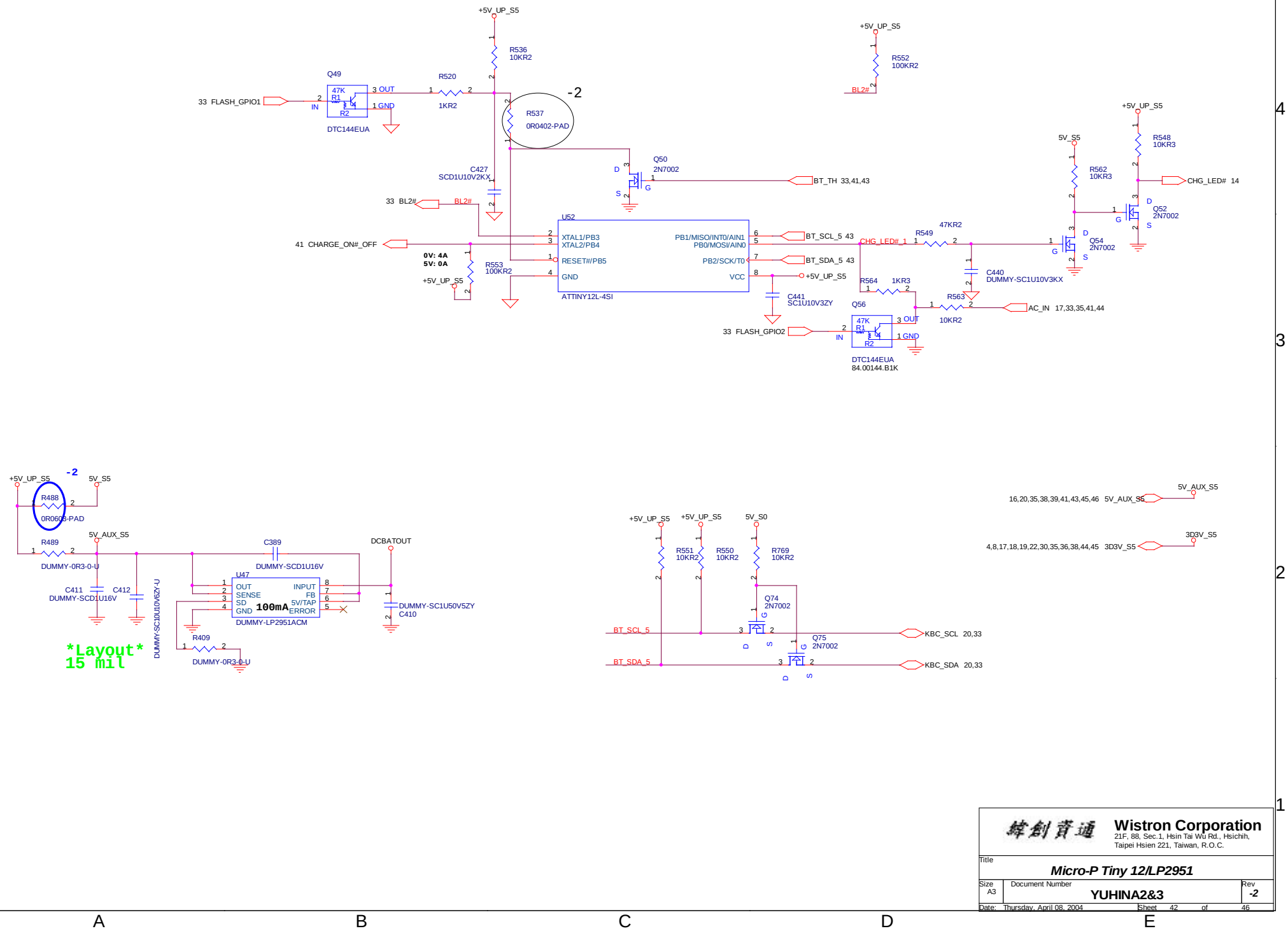

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	***Micro-P Tiny 12/LP2951***		
Size A3	Document Number **YUHINA2&3**		Rev **-2**
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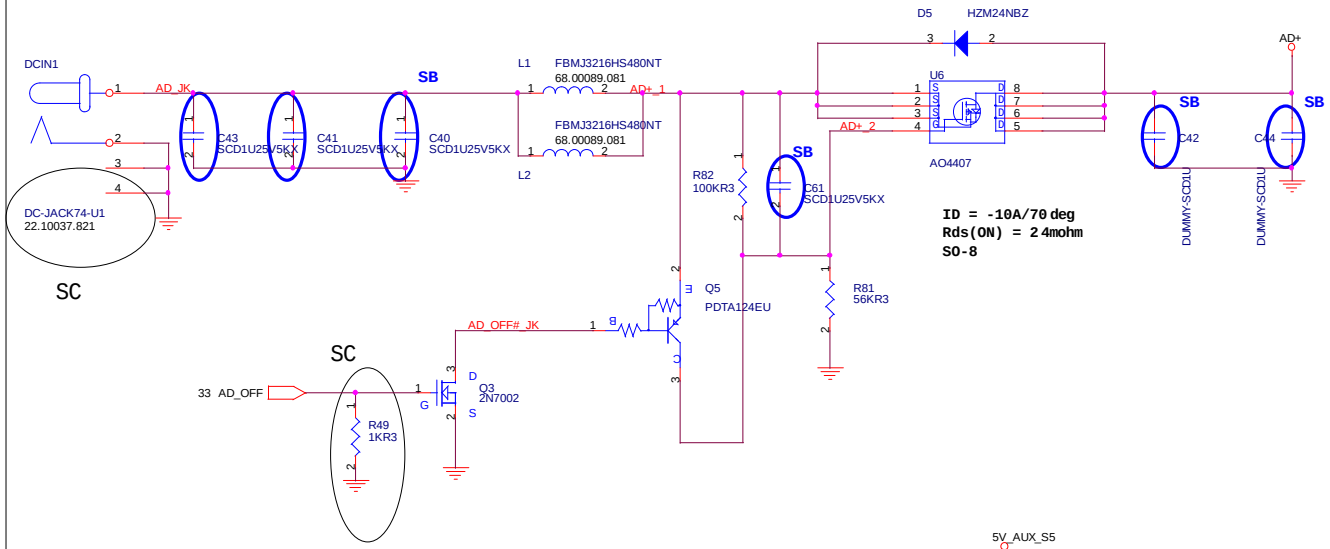
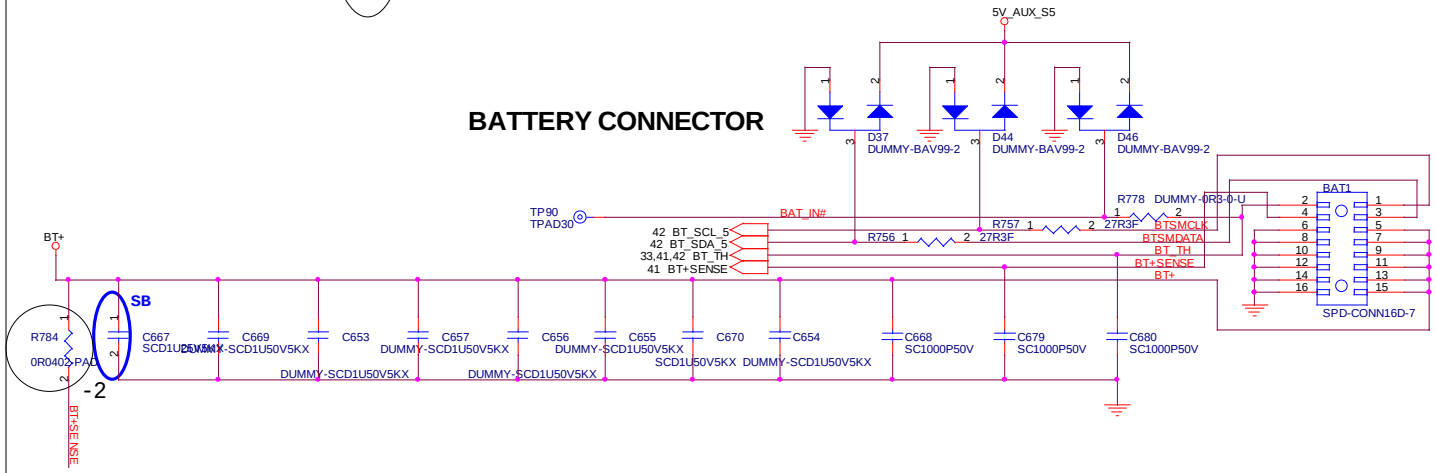
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



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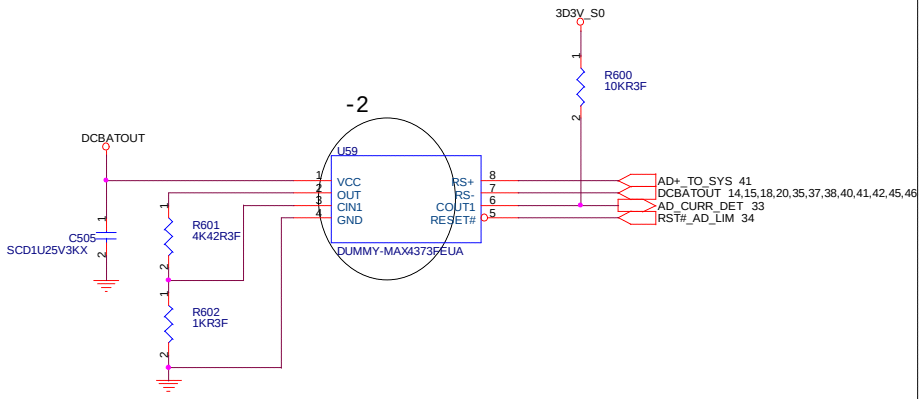
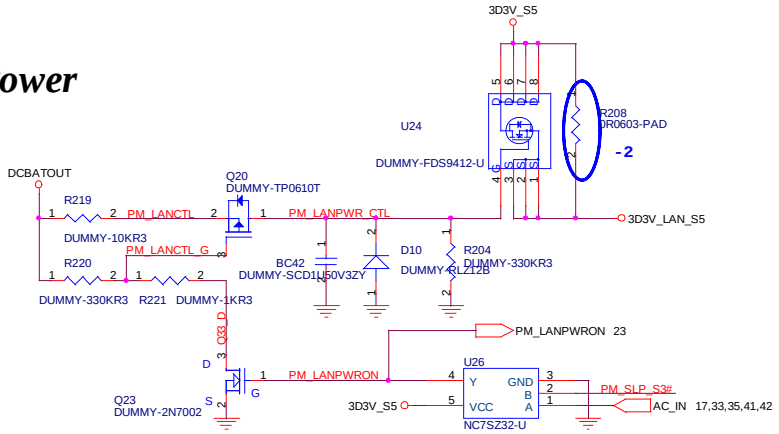
Title: *AD/BATT CONN*		
Size: A3	Document Number: YUHINA2&3	Rev: -2
Date: Thursday, April 08, 2004	Sheet 43 of 46	

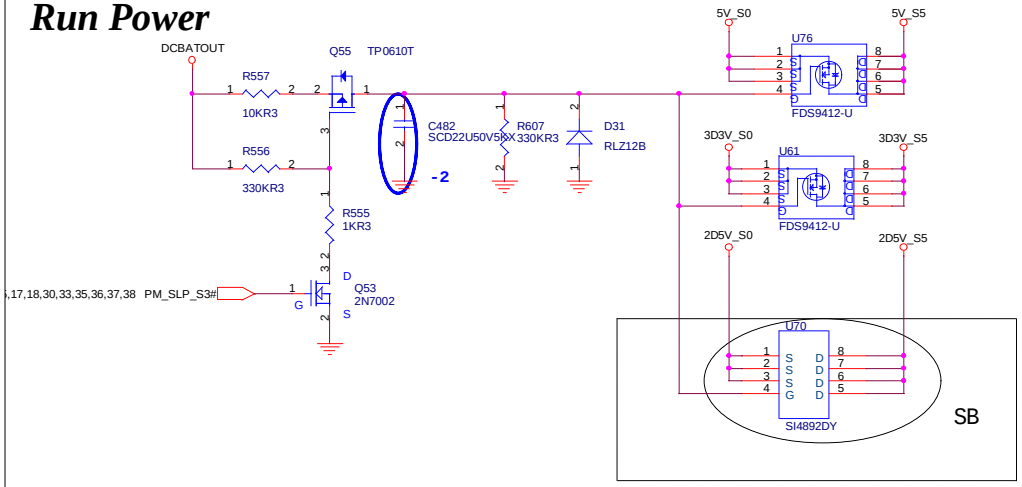


Check Setting Va lue(6.5A)

LAN Power

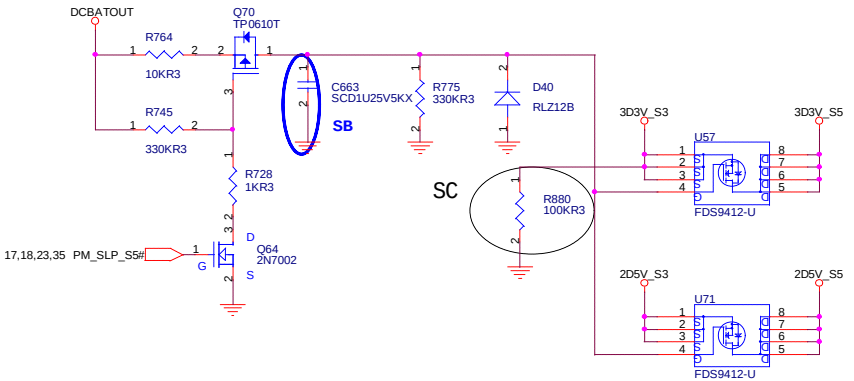


Run Power

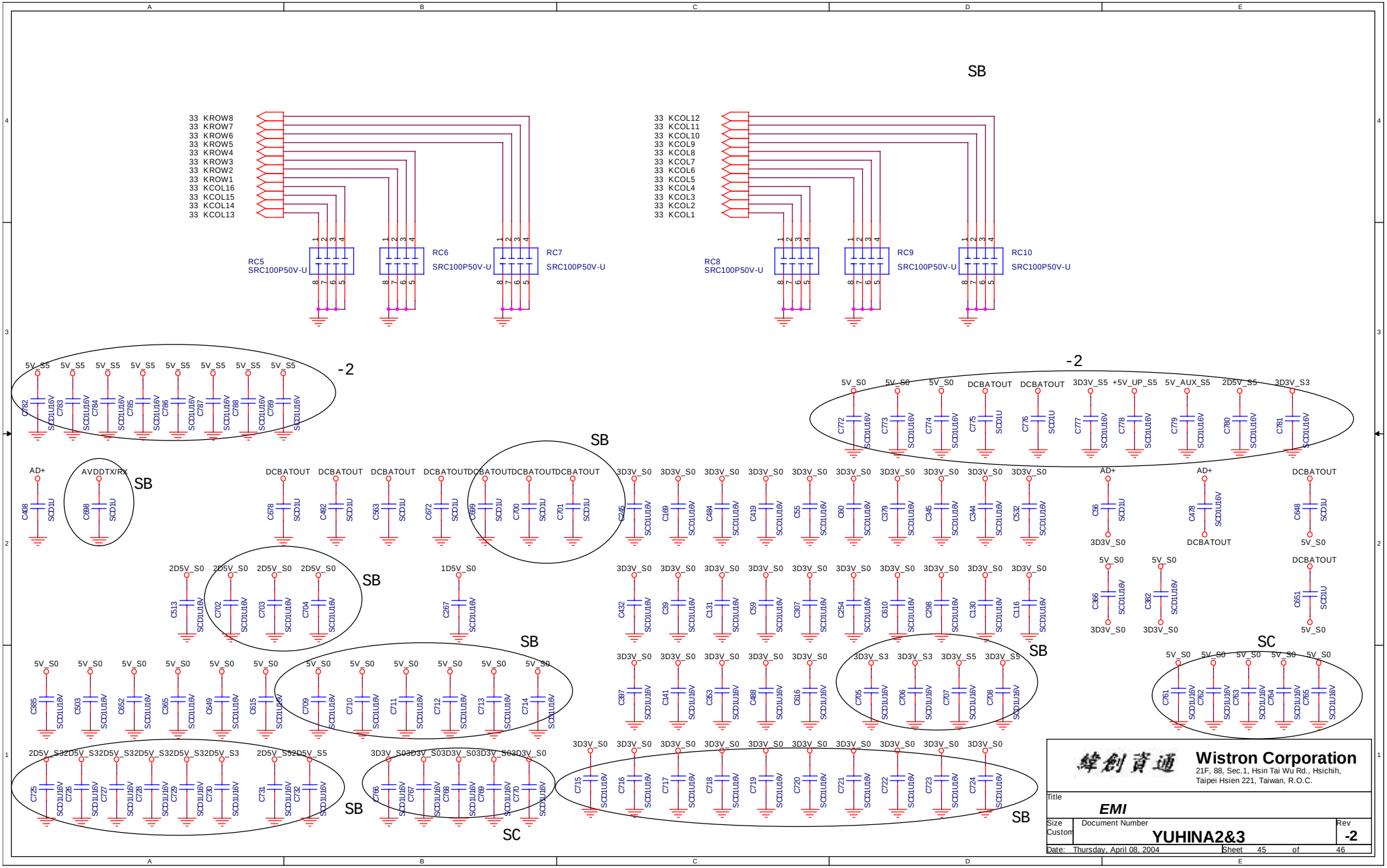


Suspend Power

Support standby wakeup LAN only



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***PWRPLANE&RESETLOGIC***	
Size A3	Document Number YUHINA2&3	Rev -2
Date: Thursday, April 08, 2004	Sheet 44 of 46	


SB
33 KROW8
33 KROW7
33 KROW6
33 KROW5
33 KROW4
33 KROW3
33 KROW2
33 KROW1
33 KCOL16
33 KCOL15
33 KCOL14
33 KCOL13
RC5 SRC100P50V-U
RC6 SRC100P50V-U
RC7 SRC100P50V-U
33 KCOL12
33 KCOL11
33 KCOL10
33 KCOL9
33 KCOL8
33 KCOL7
33 KCOL6
33 KCOL5
33 KCOL4
33 KCOL3
33 KCOL2
33 KCOL1
RC8 SRC100P50V-U
RC9 SRC100P50V-U
RC10 SRC100P50V-U
-2
5V_S5
SCD1U16V
C782 C783 C784 C785 C786 C787 C788 C789
-2
5V_S0
DCBATOUT
3D3V_S5
+5V_UP_S5
5V_AUX_S5
2D5V_S5
3D3V_S3
SCD1U16V
SCD1U
C772 C773 C774 C775 C776 C777 C778 C779 C780 C781
AD+
AVDDTX/RX
SB
C408 C688
SCD1U
DCBATOUT
C678 C482 C553 C672 C599 C700 C701
3D3V_S0
SCD1U16V
C245 C189 C494 C419 C55 C60 C379 C345 C344 C532
AD+
C56
3D3V_S0
AD+
C478
DCBATOUT
DCBATOUT
C648
5V_S0
2D5V_S0
1D5V_S0
C513 C702 C703 C704 C267
3D3V_S0
C432 C39 C131 C59 C307 C254 C610 C298 C130 C116
5V_S0
C366 C382
3D3V_S0
DCBATOUT
C651
5V_S0
SC
5V_S0
C385 C503 C652 C365 C649 C615 C709 C710 C711 C712 C713 C714
3D3V_S0
C397 C141 C353 C488 C616
3D3V_S3
C705 C706
3D3V_S5
C707 C708
C761 C762 C763 C764 C765
2D5V_S3
2D5V_S5
C725 C726 C727 C728 C729 C730 C731 C732
3D3V_S0
C715 C716 C717 C718 C719 C720 C721 C722 C723 C724
3D3V_S0
C766 C767 C768 C769 C770
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
EMI
Size Custom
Document Number
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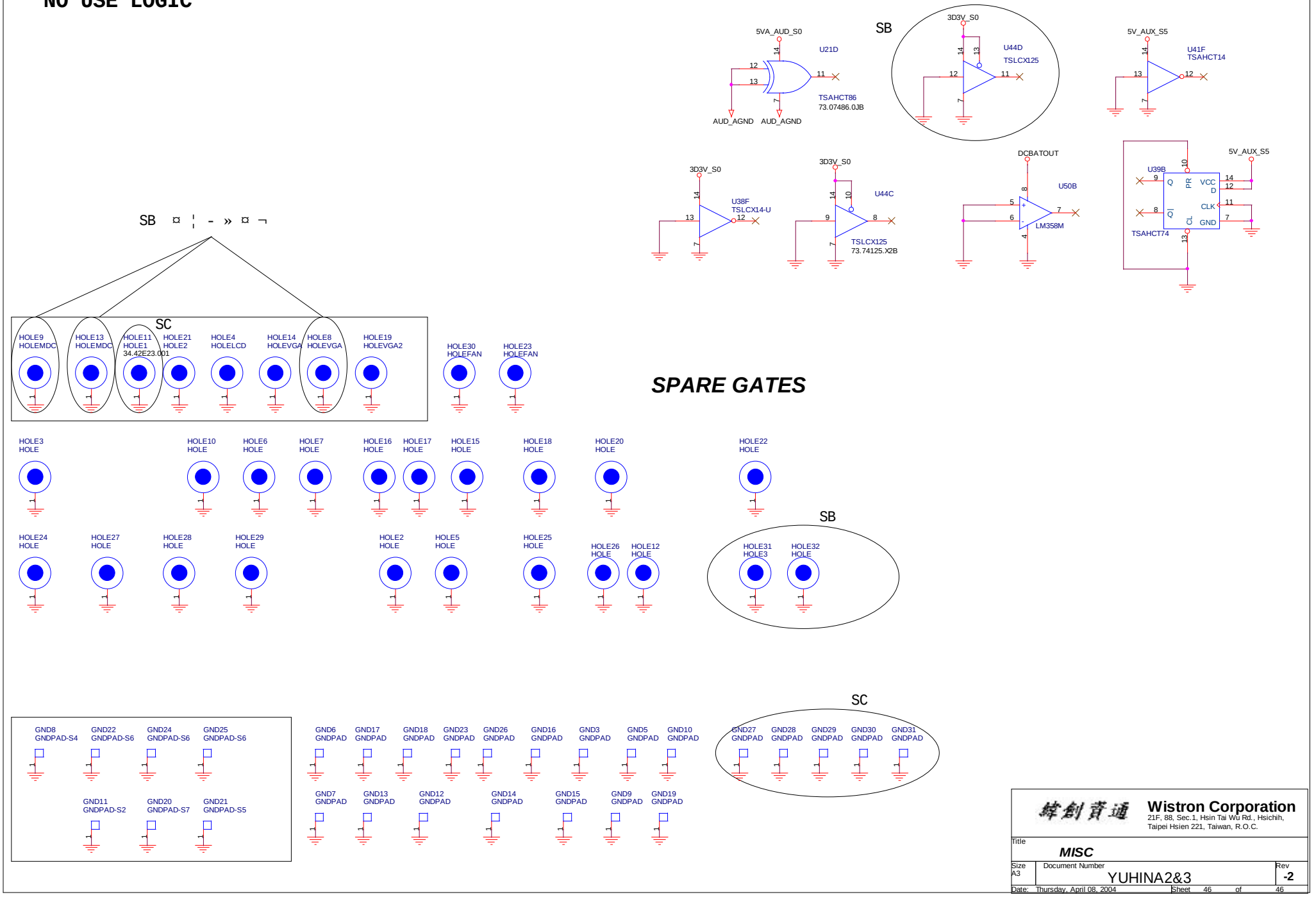
NO USE LOGIC



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Title: ***MISC***

Size	Document Number	Rev
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